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Do You Know How Much Capacitance Do You Really Get?

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INTRODUCTION

- A Real-life Scenario
- The Problem
- The Reasons
- Does It Matter?
- Possible remedies
- Conclusions

A Real-Life Scenario

- You purchase a 1uF +-20% ceramic capacitor.
- When it comes in, you measure it: it reads 0.6 uF.
- You send it back to the vendor for retesting.
- It comes back from the vendor: they say the part is in spec.
- You measure it again, you still get 0.6 uF.
- You check the measurement setups at both ends with precise reference pieces and conclude that measurements at both ends were correct.

How is this possible?

So What Is Going On?

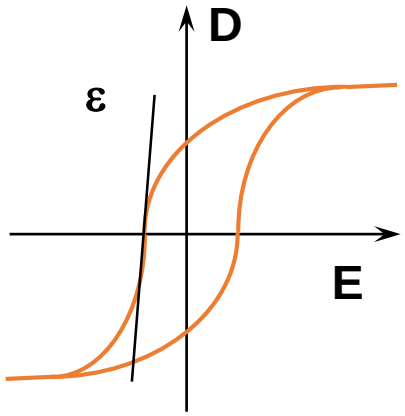
To get a clue, we need to look at the way how the measurements are done.

- Vendors use standardized measuring conditions: impedance bridge, source voltage of 1Vrms or 0.5Vrms with 100 or 120Hz frequency. *First hint: a typical capacitor at the measurement frequency is high impedance: most of the source voltage appears across the capacitor.*

- You more likely use a small pcb as test fixture and a VNA with 0dBm source power at frequencies above 1 kHz. *Second hint: in VNA measurements and in typical bypass applications the voltage across the capacitor is single or at most double digit mV.*

MLCC Material and Construction

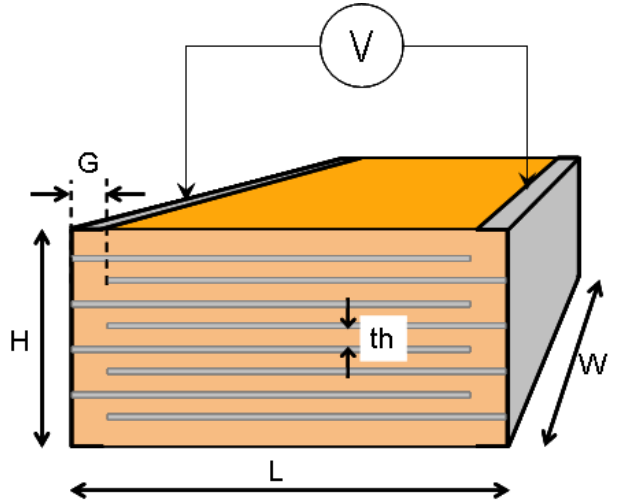
$$D = \varepsilon E$$



Class II and higher ceramic materials are ferroelectric

Ferroelectric materials have saturating hysteretic D-E curves

ε and C are voltage dependent!



Layer count

N = H/th

$$C = \varepsilon_0 \varepsilon_r N \frac{W(L-2G)}{th}$$

$$E = \frac{V}{th}$$

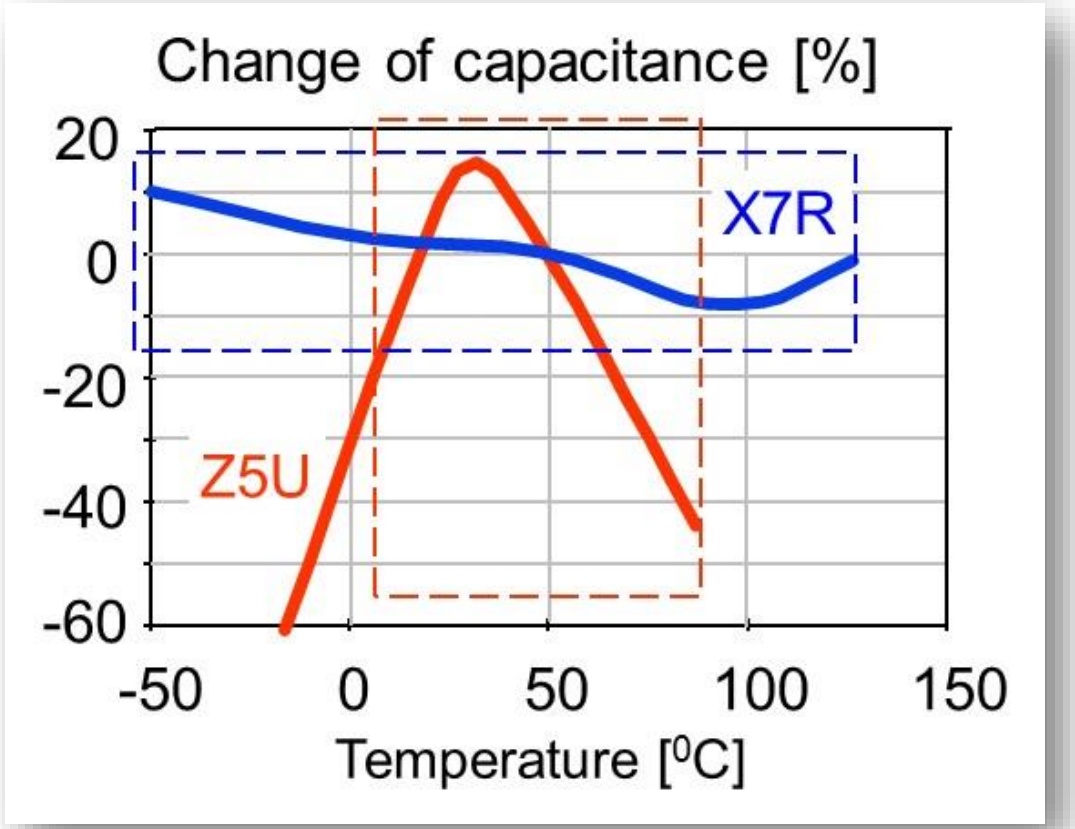
Effect of Temperature on MLCC Capacitance

EIA Class II and Class III ceramics

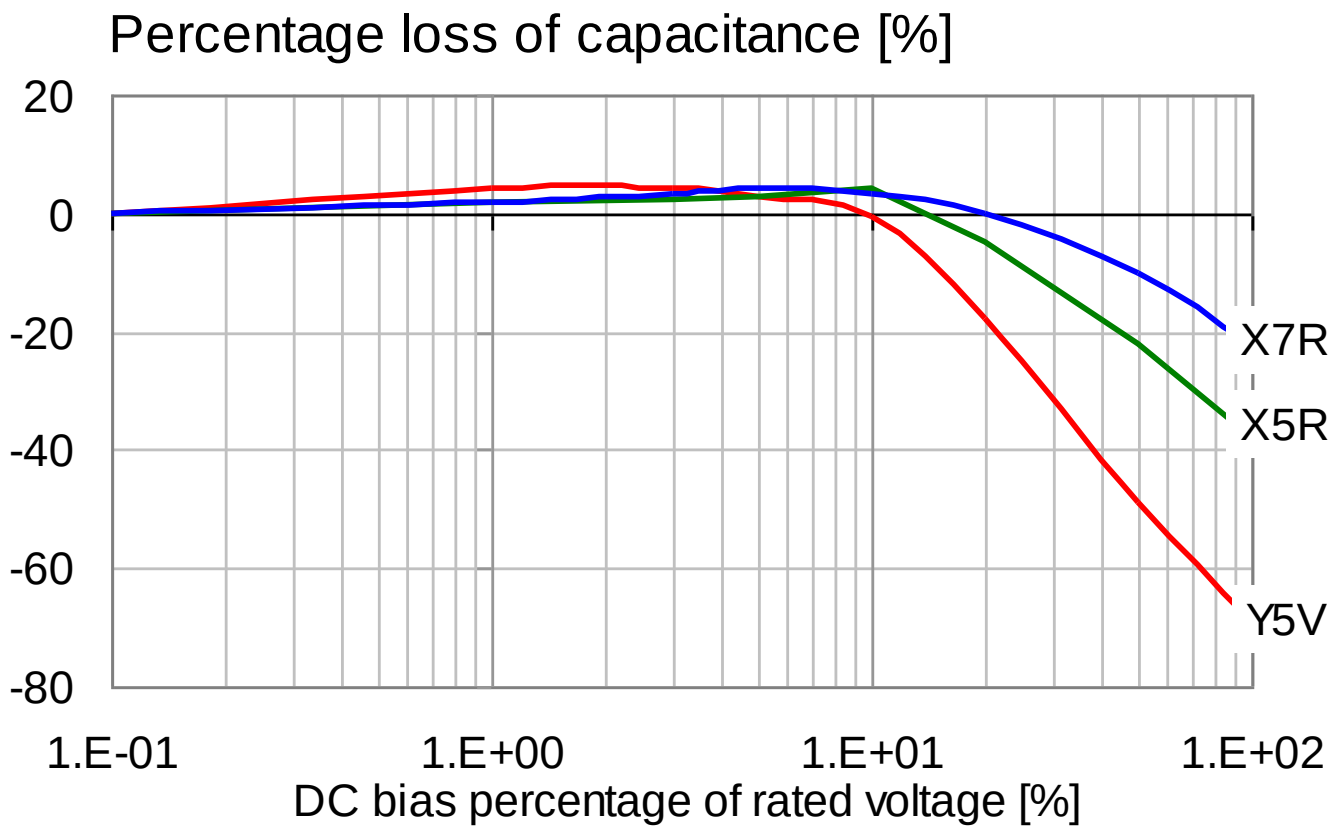
First character:
Z: + 10C
Y: - 30C
X: - 55C

Second character:
2: + 45C
4: + 65C
5: + 85C
6: + 105C
7: + 125C
8: + 150C
9: + 200C

Third character:
F: +- 7.5%
P: +- 10%
R: +- 15%
S: +- 22%
T: + 22 / - 33%
U: + 22 / - 56%
V: + 22 / - 82%



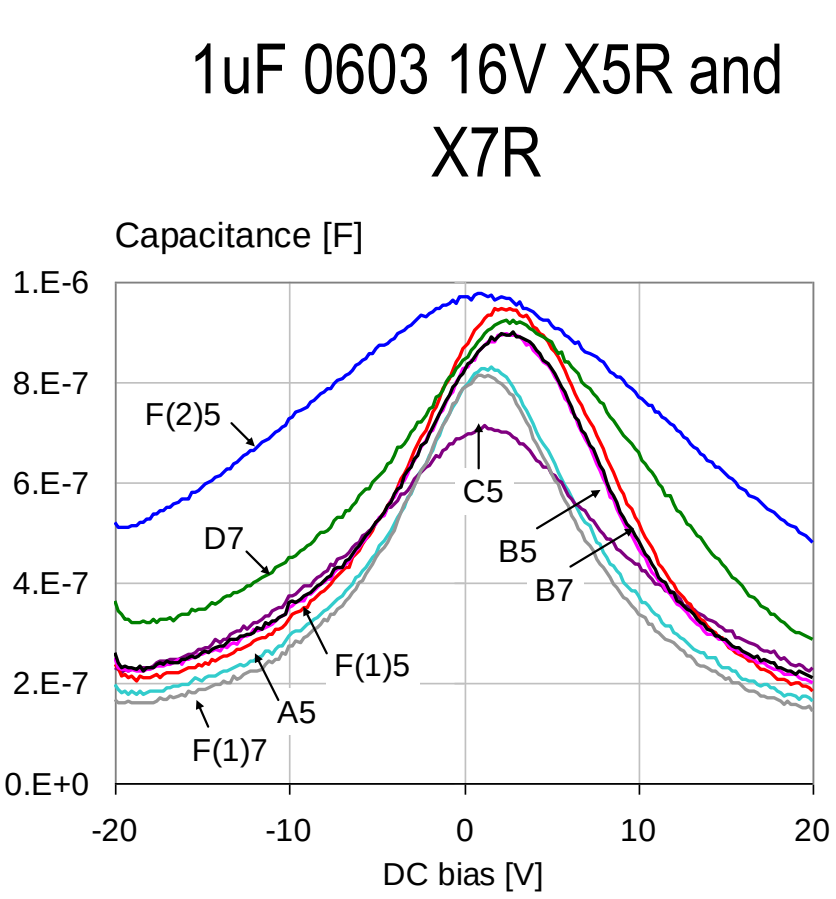
DC Bias Dependence (Old School Info)

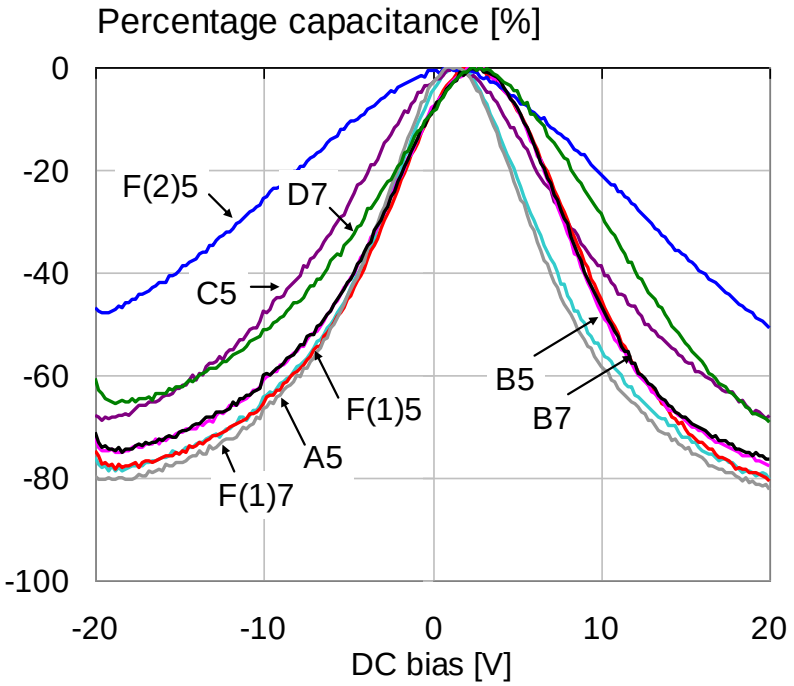


For some time, it was a common assumption that X7R MLCCs had less DC bias sensitivity than X5R parts.

But lately…

X5R vs X7R at 10mV AC



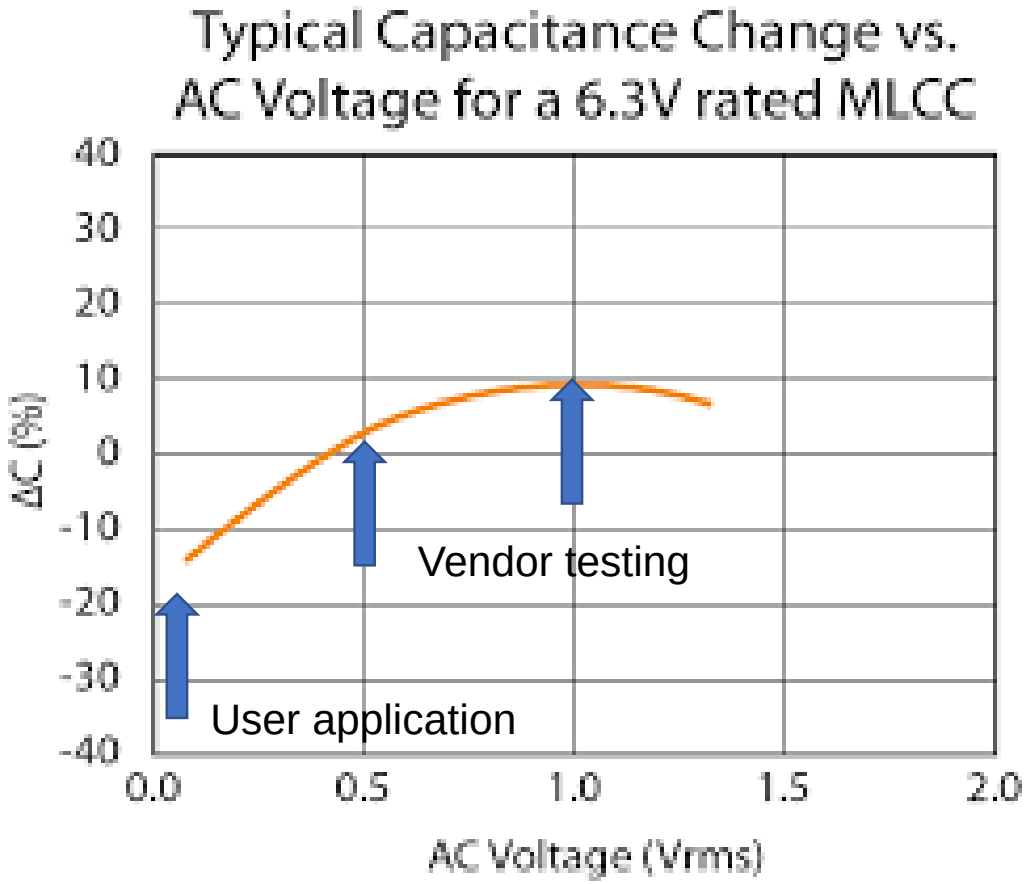


Samples from Vendors A,B,C,D,F

Last digit refers to X5R or X7R

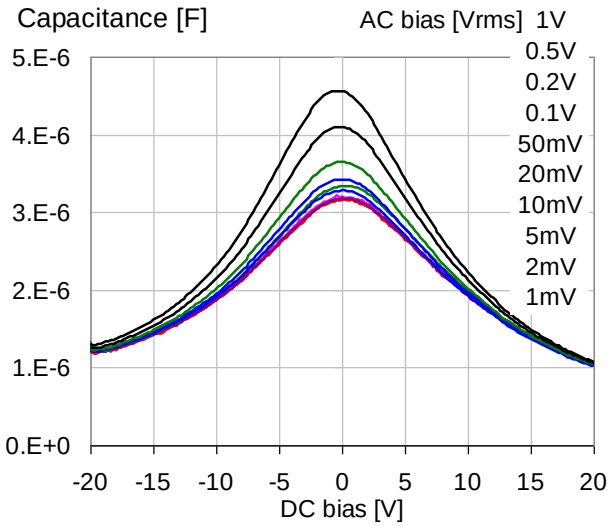
For more info see http://www.electrical-integrity.com/Paper_download_files/DCE11_200.pdf

AC Bias Dependence: The Problem

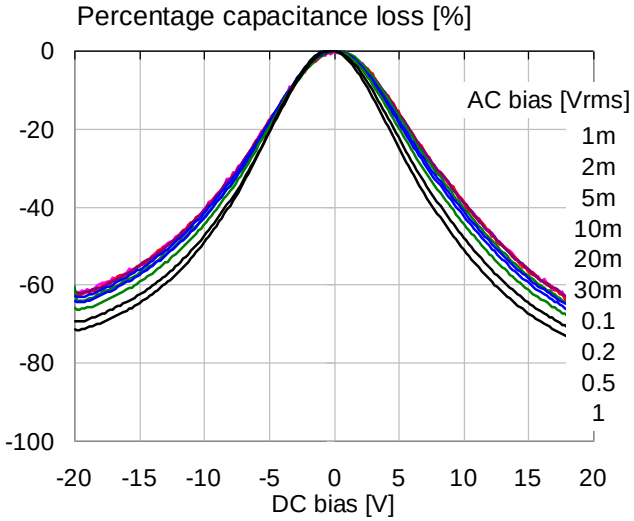


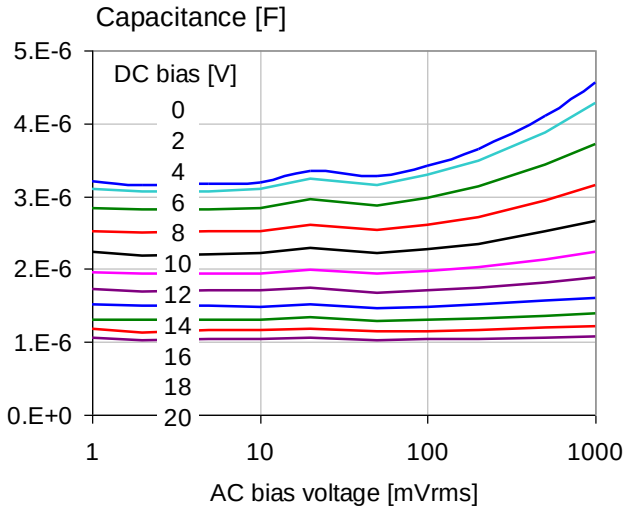
Testing and typical usage apply very different AC levels.

AC Bias Dependence



4.7uF 0805-size 16V X5R parts from Vendor F



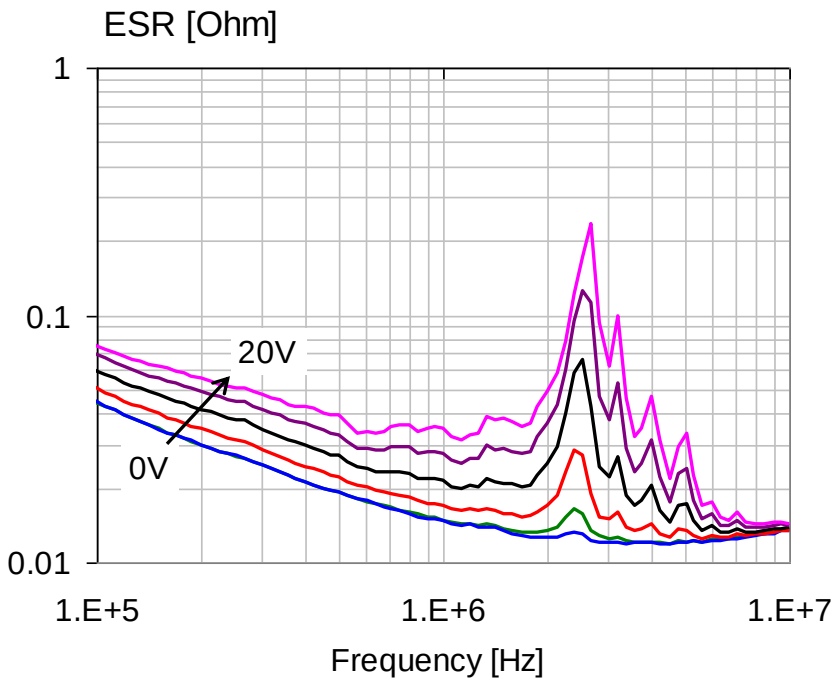


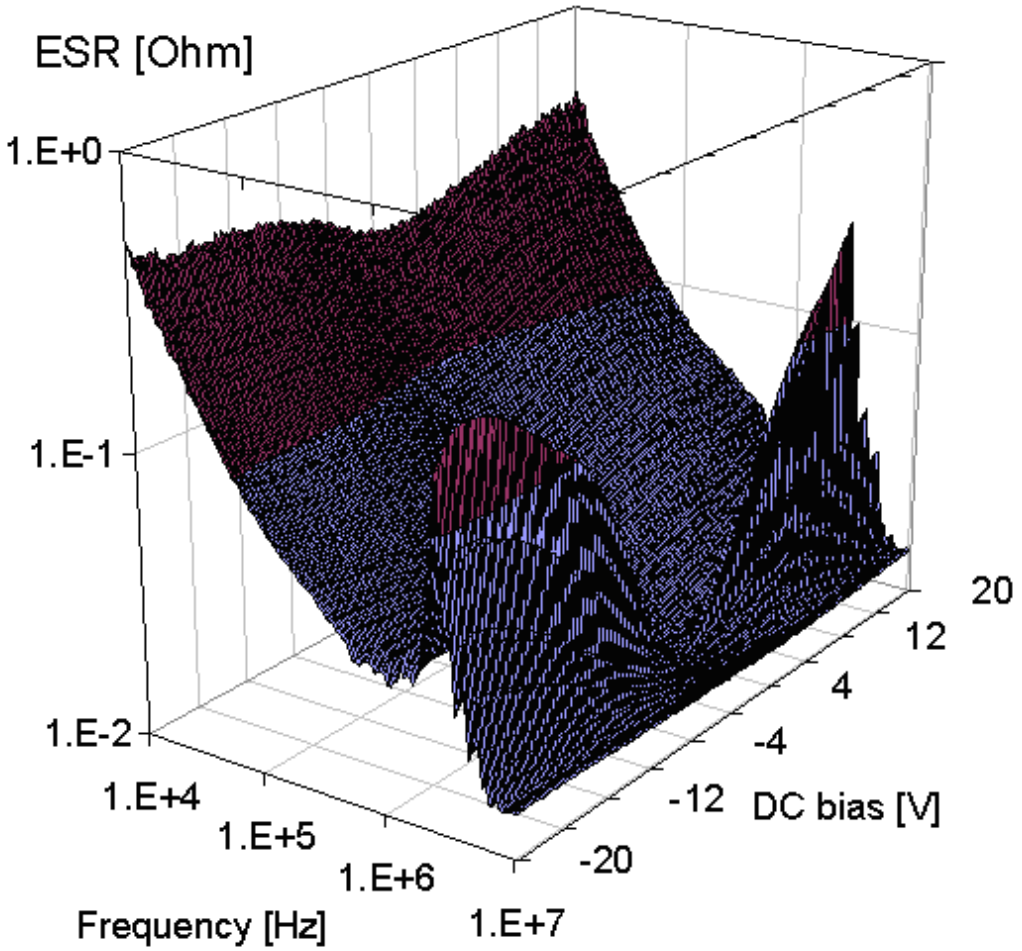
High AC bias increases capacitance at low DC bias.

At high DC bias the AC bias sensitivity is lower.

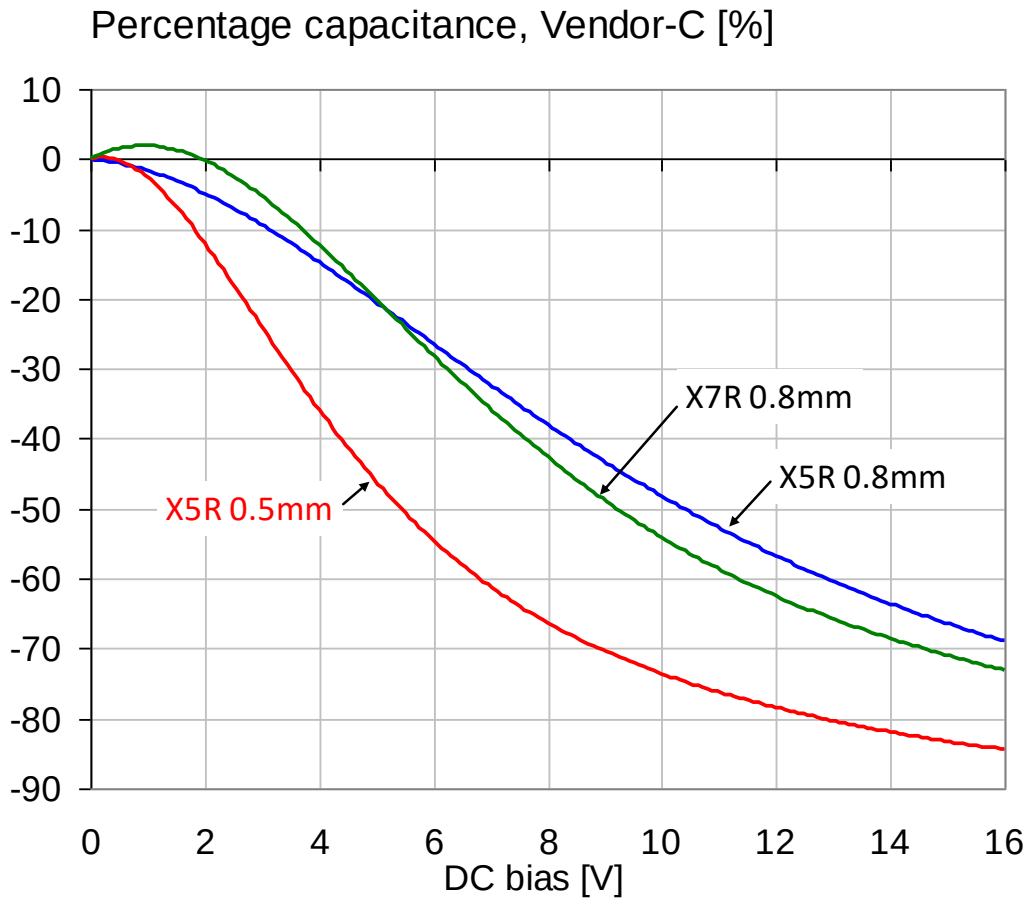
ESR and ESL vs Bias

- ESR does not change above SRF
- ESR increases below SRF as C drops
- Piezo effect shows up with increasing bias
- ESL shows no measurable difference





Beware of Details



- Sensitivity vs. body height
  - Data from vendor
- Lower body height comes with higher sensitivity

OK, Less Capacitance, So What?

In SI (less of an issue)

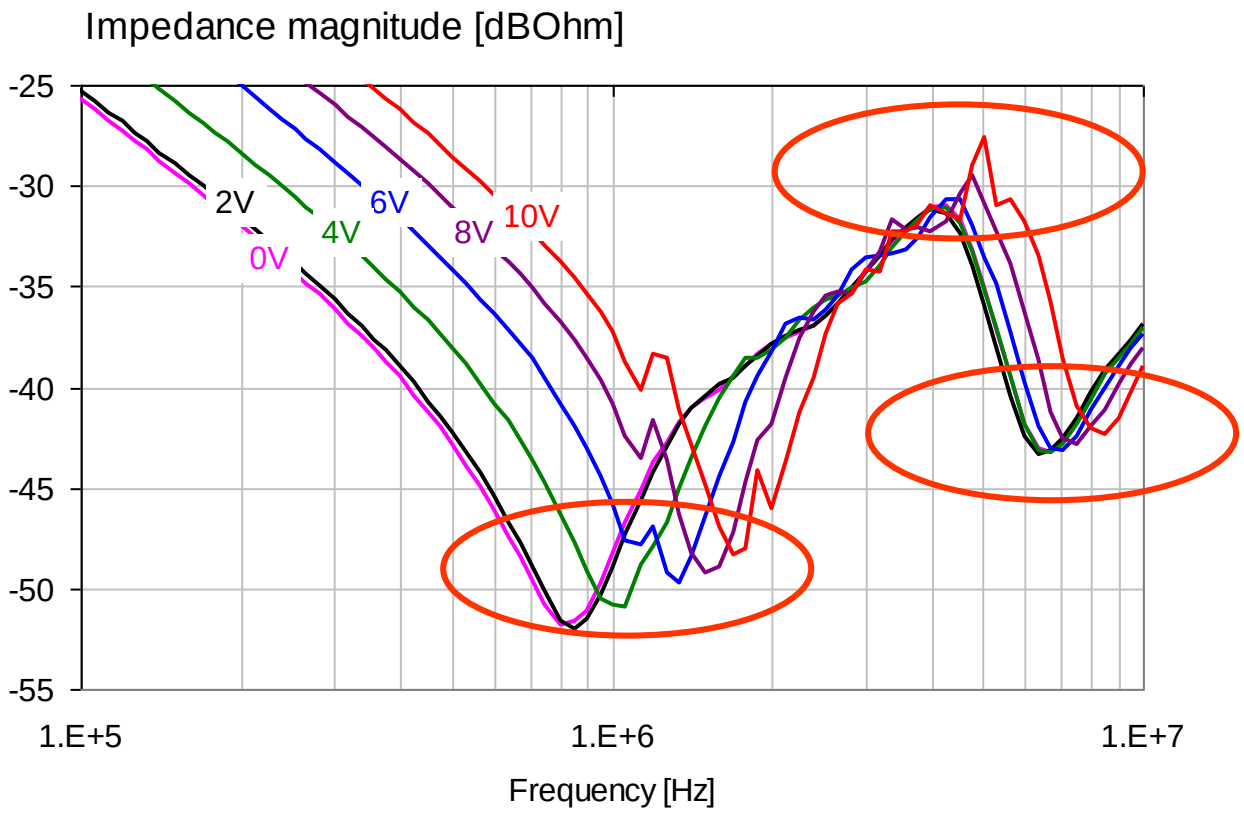
* If OK for the design, just oversize the capacitance (worst case: by 6x)
* Design could become space limited
* In differential DC block the two legs may become unbalanced at low frequencies

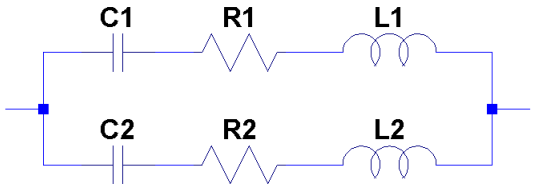
In PI (much more serious)

* Results in more droop (in case of single capacitor bank)
* Results in peaking (more noise)
* May result in current amplification, increased dissipation

OK, Less Capacitance, So What?

1uF 0603-size 16V X7R part from Vendor-D and 47uF 1206-size 6.3V X5R part from Vendor-E





All three resonances shift.

For more info:
http://www.electrical-integrity.com/Paper_download_files/DC16_Paper_ElectricalAndThermalConsequencesOf_Choi.pdf

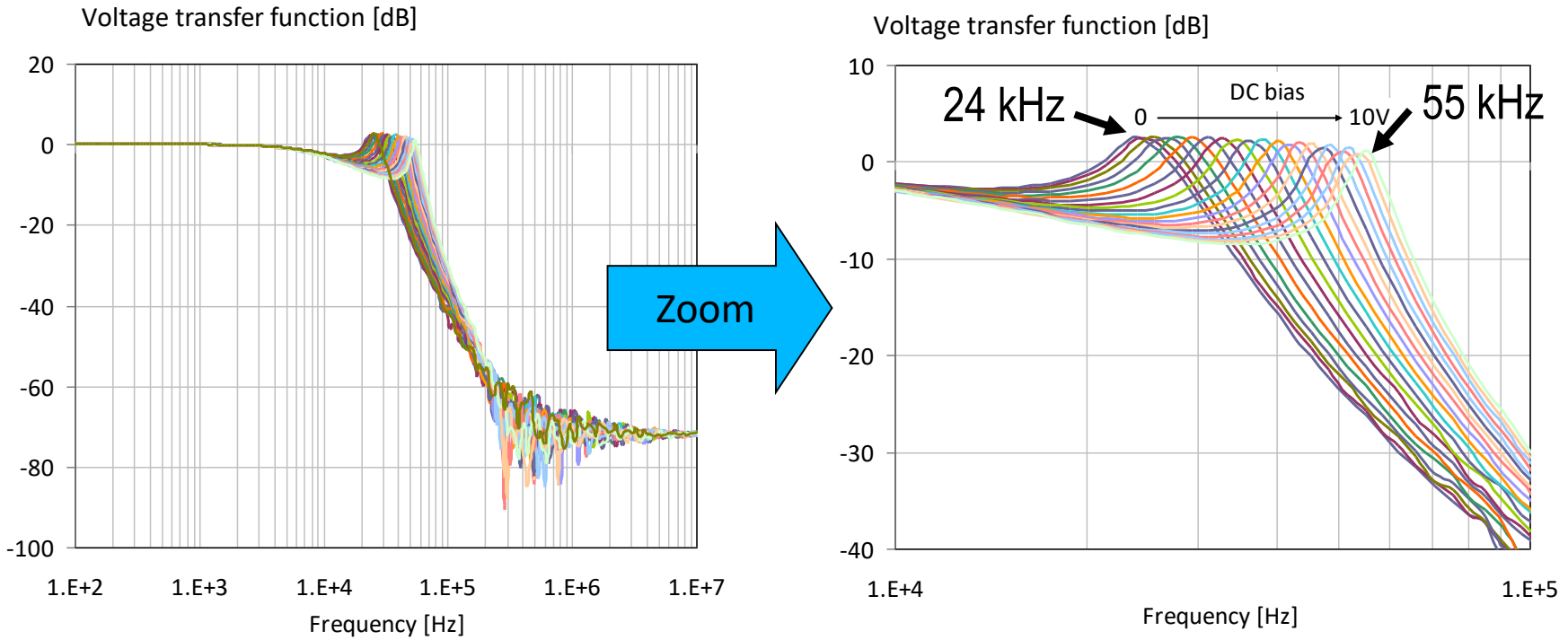
Filter Response vs. DC Bias Voltage

No DC current bias through L1

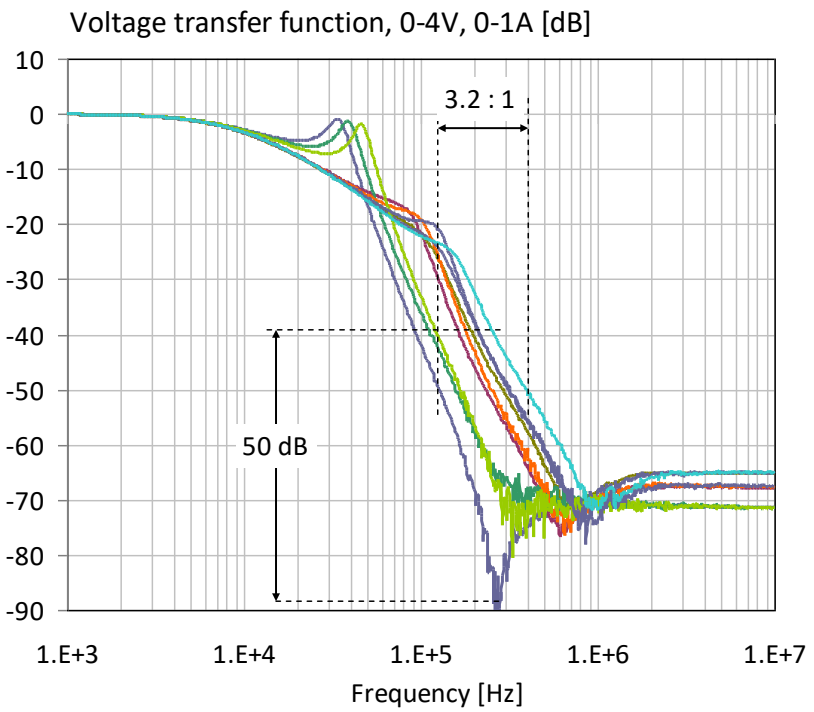
No change below 10 kHz and above 1 MHz

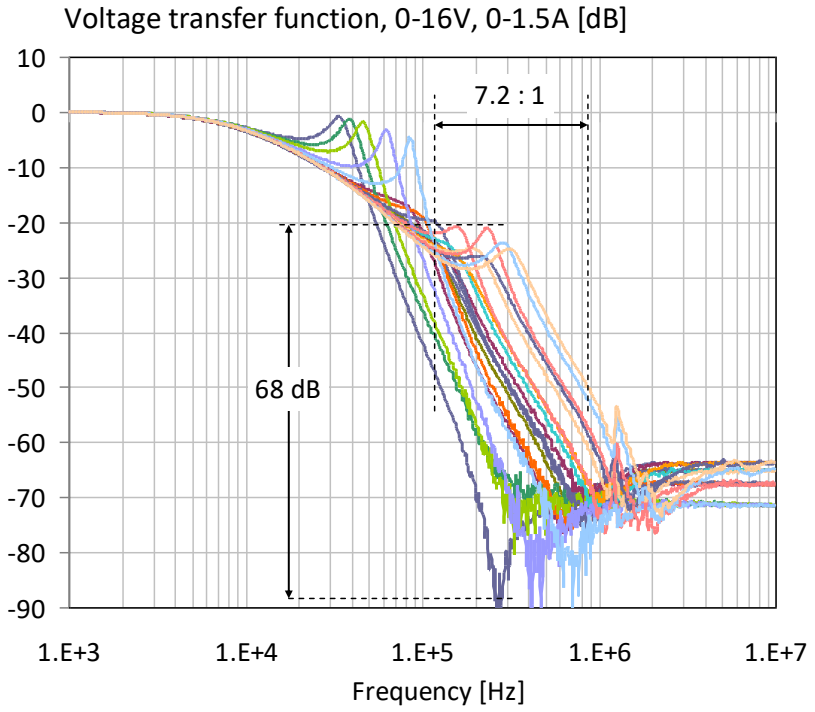
No change in peaking

Peak frequency and cut-off frequency increases with increasing bias



Change Due to DC Bias Voltage and Current





For more info see http://www.electrical-integrity.com/Paper_download_files/DC19_Tutorial_SLIDES_HowToDesignGoodPDNFilter.pdf

What Else May Change the Capacitance

	Percentage range [%]	Relative multiplier
Initial tolerance	+-10	0.9 … 1.1
Temperature effect	+-15	0.85 … 1.15
DC bias effect	+0 -70	0.3 … 1
AC bias effect	+0 -30	0.7 … 1
Aging (over 3 years)	+0 -7.5	0.925 … 1

When we multiply the worst-case contributors, we get 0.9*0.85*0.3*0.7*0.925 = 0.15, which means in worst case *instead of 1uF we have only 0.15uF capacitance*.

Does This Happen In All Capacitors?

Luckily, NO.

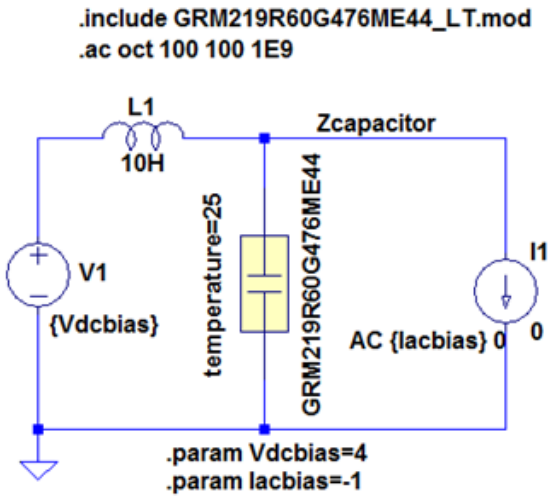
This happens in high Dk MLCCs

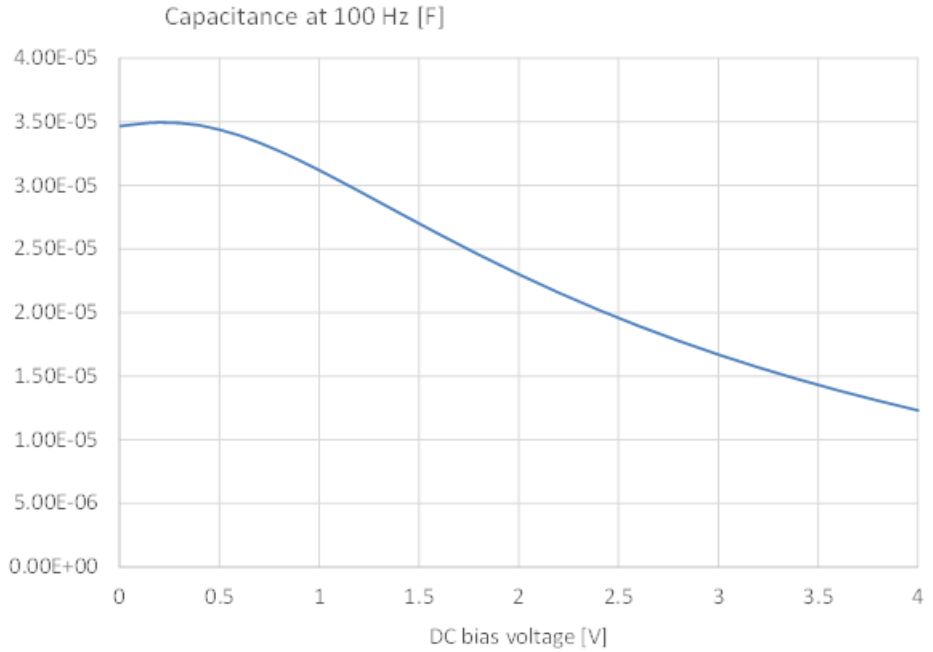
It does not happen in

* Low Dk MLCCs (COG/NPO), but we don't get high density either
* Electrolytics
* Tantalum
* Polymer
* Film

How To Simulate

* S-parameter models don't easily scale
* SPICE equivalent circuits scale easily, but in complex models, scaling is tricky due to multiple Cs describing a single device
* Best option: dynamic models (available for most Murata MLCCs)





For more info on dynamic models: http://www.electrical-integrity.com/Quietpower_files/QuietPower-36.pdf

How To Mitigate

If the DC-AC bias effects have to be reduced, consider to

* Create circuits, which are less sensitive to capacitance variations
* Check carefully bias curves (if available) and select ‘better’ parts
* Avoid using MLCC parts with the highest capacitance density
* Avoid using MLCCs

Conclusions

* DC and AC bias effect can reduce MLCC capacitance substantially
* Total capacitance loss can be up to 80-90%
* Capacitance loss can increase droop, resonance peaks and degrade filter performance

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