M1489/M1487: 486 PCI Chip Set

Features

M1489 (Cache-Memory PCI controller)
M1487 (ISA Bus Controller)

Supported CPUs
- Supports AMD 486D4 and X5, Intel 486, P24T, P24D, DX4, SL-Enhanced, Cyrix M7, UMC U5 and AMD AM486DXL CPUs in 25, 33, 40, 50, 66, 100 and 133 MHz 3V/5V CPU interface
- Supports CPU L1 writeback
- Supports Cyrix's linear addressing mode

L2 Cache Controller
- Write Back cache with standard SRAM
- 8 Tag Bits, always force Dirty or 7 Tag Bits, 1 Dirty bit
- Supports cache size of 128K to 1M with 32Kx8, 64Kx8, 128Kx8
- Supports 2-1-1-1 read burst timing
- Write hit 0 wait support

DRAM Controller
- Supports 5V/3V EDO DRAM
- Flexible DRAM type & Timing support
- Supports up to 128M bytes, 4-bank DRAM size
- Supports hidden refresh and RAS only normal refresh

Built in RTC & KBC
- Built in 128 byte RTC & MC14069
- Built in KBC & 7406

Built in IDE Controller
- Dedicated IDE pins, concurrent with PCI bus
- 4x32 bits Read-Ahead buffer and Write-Post buffer support
- Supports through ATA PIO mode 3, 4 harddisk

PCI Local bus
- Synchronous 20, 25, 33 MHz PCI clock
- Supports PCI rev 2.0 with 4 PCI devices, 3 slot PCI masters, 1 slot PCI slave
- Supports 4 PCI interrupt steering input
- Supports CPU to PCI 4 layer DWord write buffer
- Supports PCI to memory 8 layer DWord write buffer
- Supports PCI parity

Power Management
- Deep Green SMM, SMI
- Suspend switch support, Green mode state is LED indicated
- CLKCTR clock generator control

Process/Packing
- M1489 0.6µ, 208-pin PQFP
- M1487 0.6µ, 160-pin PQFP

Table of Contents

Section 1: Introduction

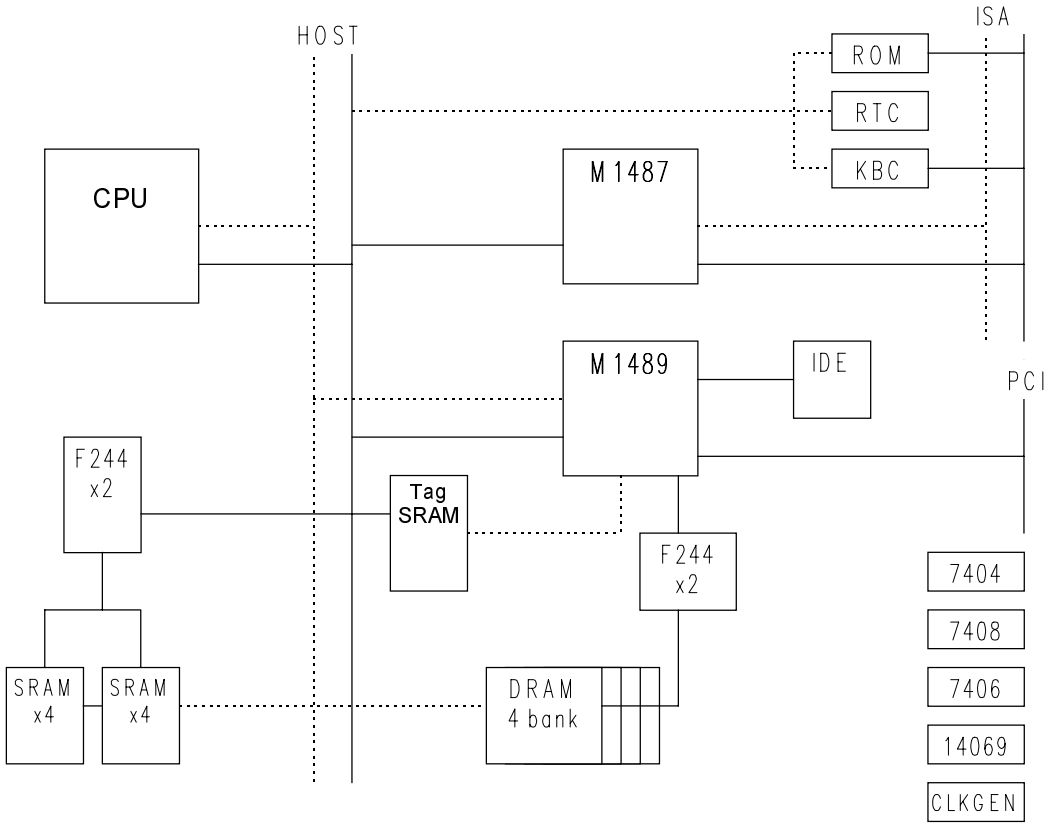
ALi's M1489/M1487 PCI chipset is the most cost effective PCI solution available. M1489/M1487 enables top-to-bottom PCI in 486 CPU systems, offering superior price/performance for mainstream PCI-ISA systems.

M1489/M1487 highly integrates the DRAM controller, L2 cache controller, Host, PCI, and ISA interface, as well as the standard ISA functions: DMA controller, interrupt controller, timer/counter, RTC (Real Time Clock), and keyboard controller. Additionally, M1489/M1487 incorporates the high performance Local Bus IDE allowing a system designer to implement Local bus IDE with no additional cost. M1489/M1487 is a highly integrated solution requiring minimized TTL components, enabling PCI-ISA designs at costs equal to or lower than comparable VL Bus designs.

M1489 (Cache Memory PCI Controller: CMP) integrates the L2 cache controller and the DRAM controller. The cache controller supports write-back cache policies and cache size from 128K to 1M byte in an interleaved or non-interleaved configuration. The DRAM controller interfaces DRAM to the Host bus, PCI bus, and Link bus. M1489 can support EDO 3/5V DRAM, standard DRAM, and flexible timing select. M1489 also integrates intelligent Host to PCI, PCI to Host buffer to achieve high performance. Also, M1489 provides the high performance Local Bus IDE interface.

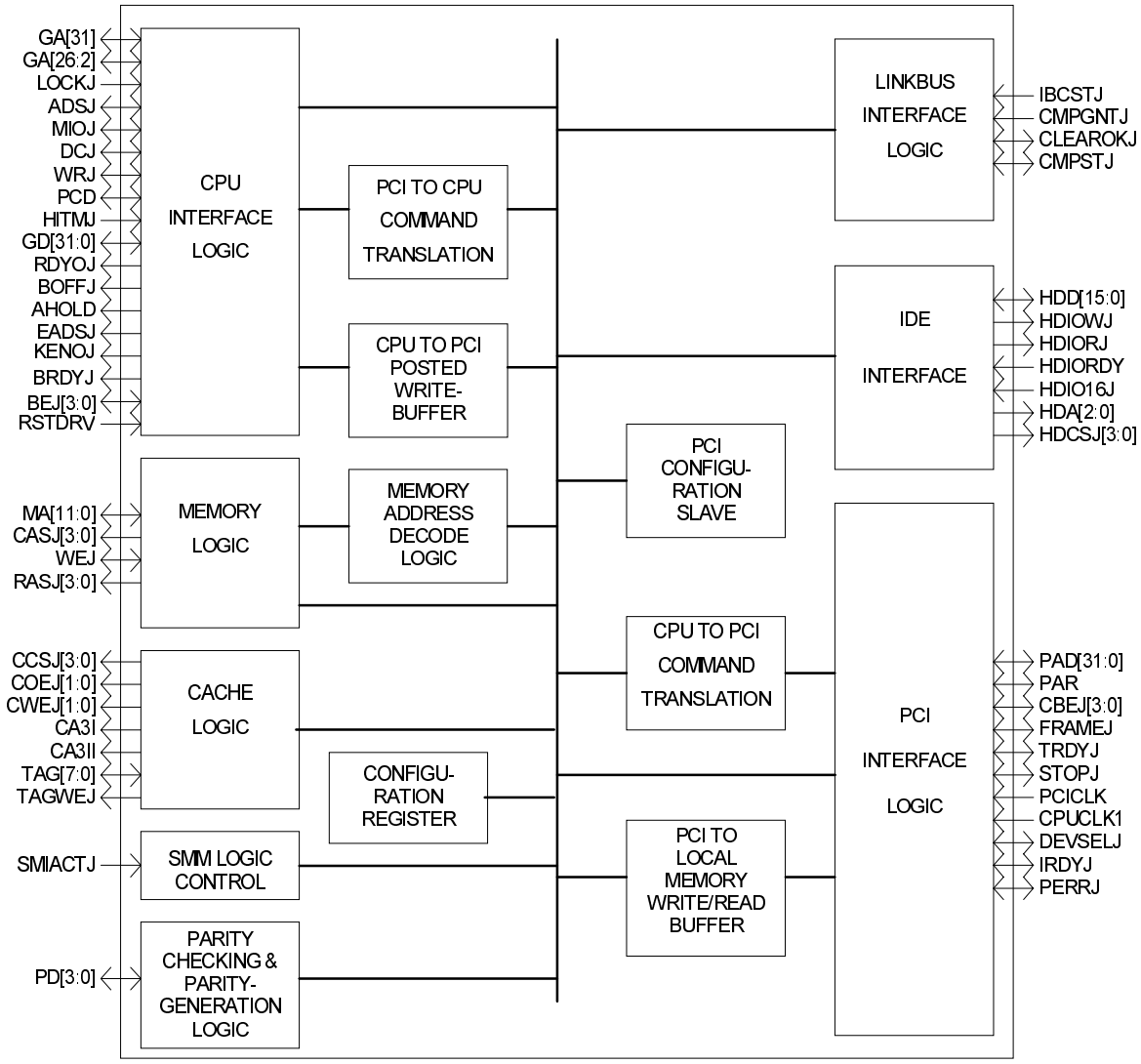
M1487 (ISA Bridge Controller: IBC) provides the bridge between the ISA bus, PCI bus, and Host bus. IBC integrates the common I/O functions found in today's ISA based systems: a seven channel DMA, two 82C59 interrupt controllers, 8254 timer/ counter, deep green function, and control logic for NMI generation. IBC also has built-in 128 bytes RTC, MC14069, KBC, and 7406. IBC also provides the decode for external BIOS.

1.2 System Block Diagram

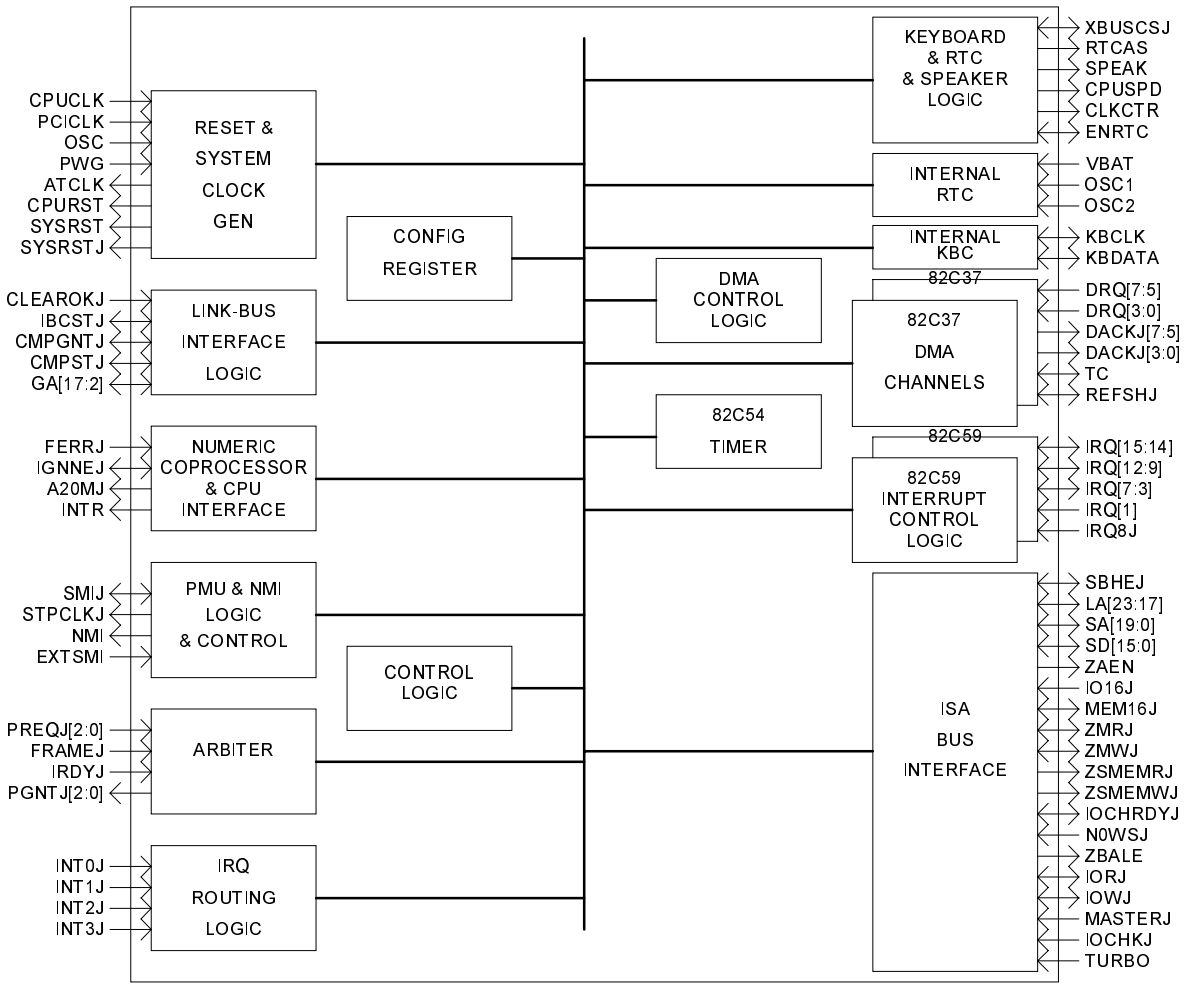


1.3 Function Description

Internal Block Diagram M1489

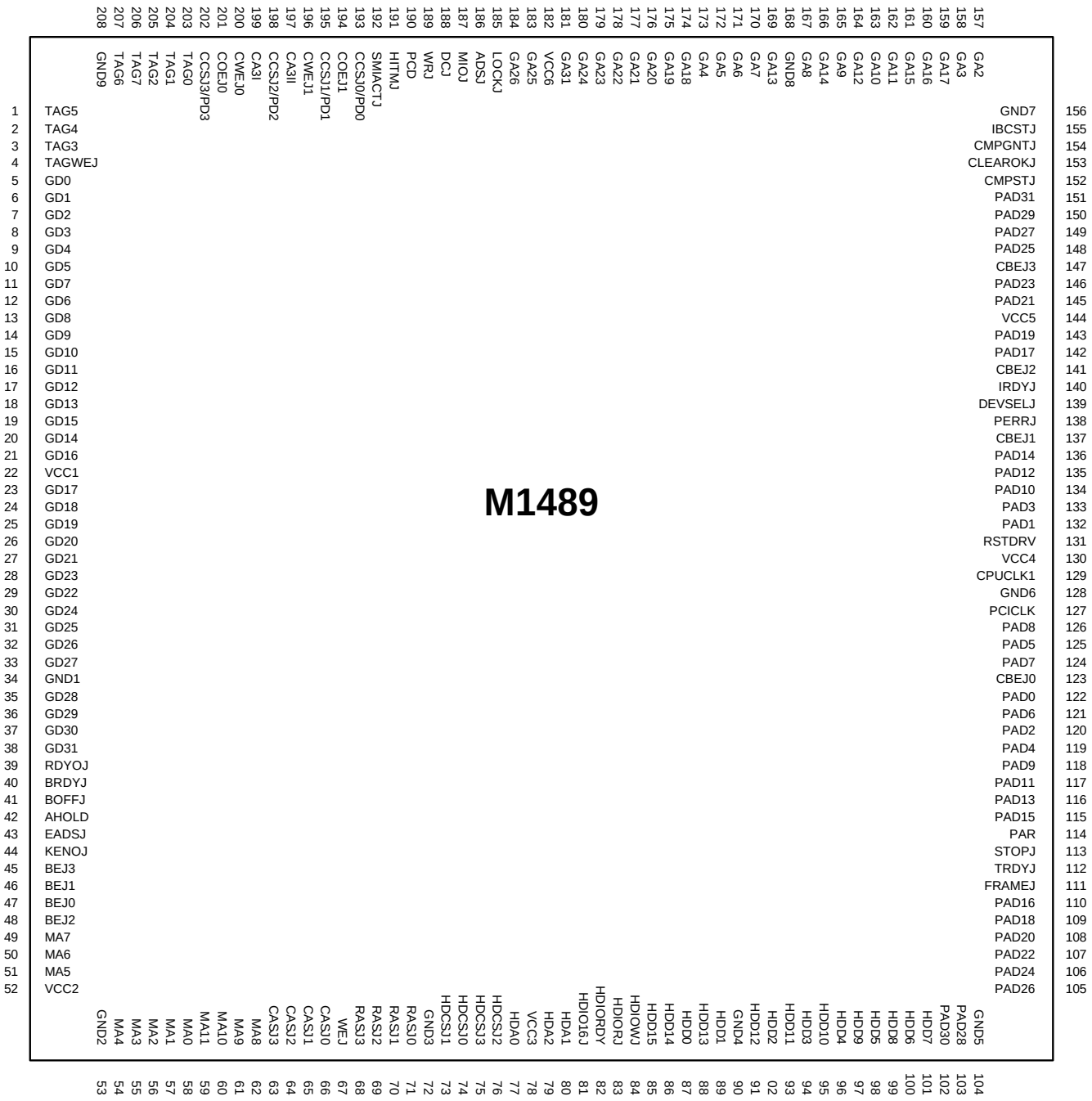


Internal Block Diagram M1487

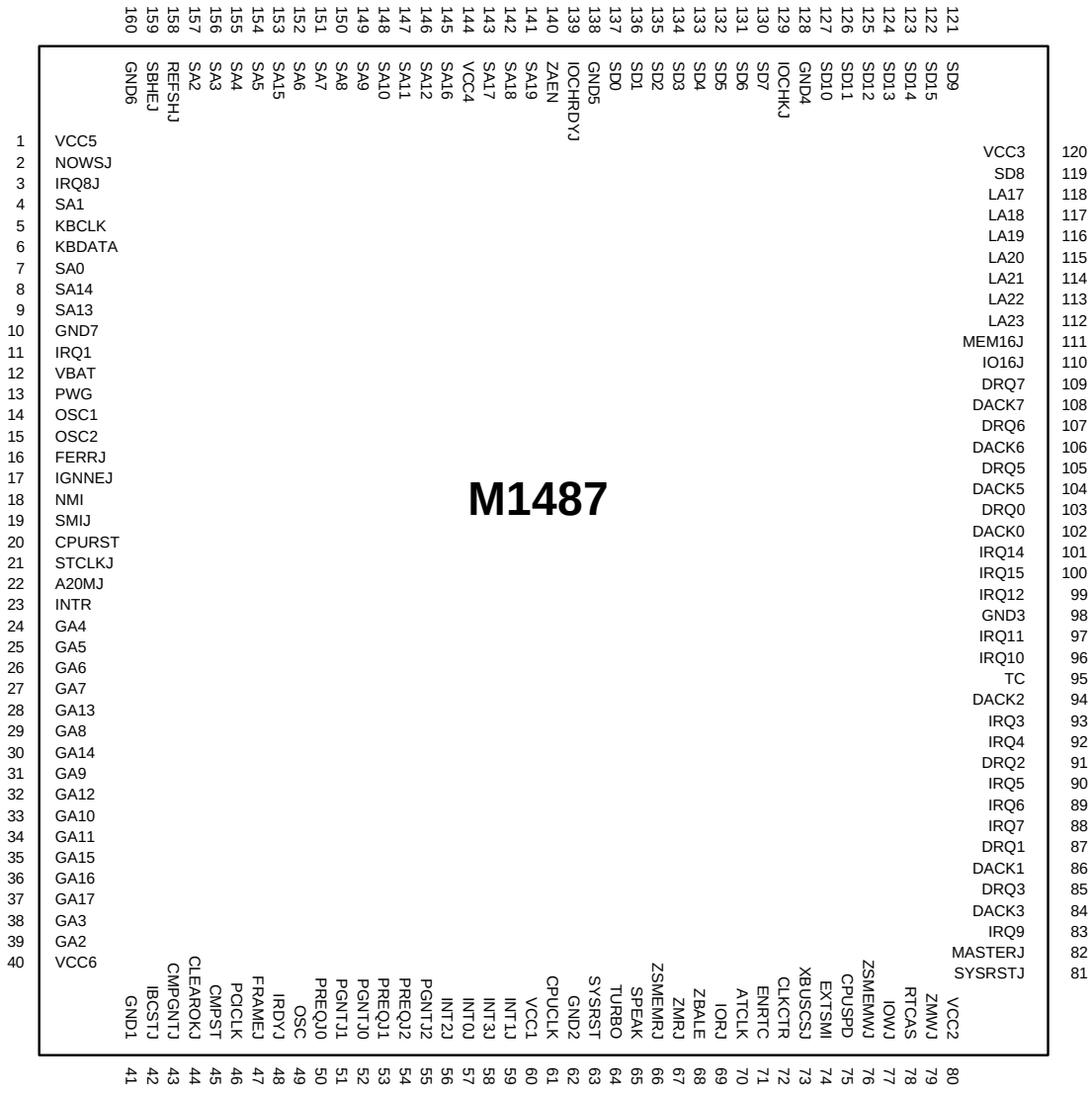


Section 2: Pin Description

2.1 Pin Diagram (M1489)



Pin Diagram (M1487)



2.2 Pin Description Table

Table 2-1. M1489 Pin Description Table

Name	Number	Type	Description
CPU Interface			
GA[31]	181	I/O	**Address 31**. This is the processor address line 31. It is used to recognize PCI or BIOS. It is input for CPU cycles and is driven low during ISA/DMA Master cycles.
GA[26:24]	184, 183, 180	I/O	**Address[26:24]**. These addresses decode the accessed targets. They are inputs for CPU cycles and is driven low for PCI/DMA/ISA Master and REFRESH cycles.
GA[23:2]	179-169, 167-157	I/O	**Address[23:2]**. These addresses are connected to CPU addresses. They decode for accessed targets. They are inputs for CPU, and are driven output for PCI/DMA/ISA Master and REFRESH cycles.
BEJ[3:0]	45,48 46,47	I/O	**Byte Enable**. These are the byte enable signals for the data bus. These signals are ignored during the local memory read access cycles, and the data of all bytes will be treated as enable to access when write. In the PCI/DMA/ISA MASTER accesses cycles, these byte enable signals will be driven by M1489 to host bus.
ADSJ	186	I/O	**Address Strobe**. The address status indicates that a new valid bus cycle is currently being driven by the CPU. In the PCI/ DMA/ ISA Master access cycles, this signal will be driven by M1489 to host bus.
MIOJ, DCJ, WRJ	187, 188, 189	I/O	**Memory or I/O, Data or Code, Write or Read**. The memory/input-output, write/read, and data/code lines are the CPU bus cycle definition pins. In the PCI/DMA/ISA Master access cycles, these signals will be driven by M1489 to host bus.
RDYOJ	39	O	**Ready Out**. The non-burst ready output indicates that the current bus cycle is complete.
BRDYOJ	40	O	**Burst Ready Out**. The burst ready output performs the same function during a burst cycle that RDYOJ performs during a non-burst cycle.
PCD	190	I/O	**Page Cache Disable**. The page cache disable pin indicates that the current CPU bus cycle is non-cacheable. This signal is not available in the Intel L1 write-back system.
LOCKJ	185	I	**Lock**. The bus lock pin indicates that the current CPU bus cycle is locked.
HITMJ	191	I	**Hit Modify**. The hit modified cache pin is asserted to indicate that a hit to a modified data cache occurred. This signal pin is only available in write-back processor system.
GD[31:0]	38~5	I/O	**Data Bus [31:0]**. These are the 32 data lines.
BOFFJ	41	O	**Backoff**. This backoff signal pin is used to force the processor floating its bus in the next clock.
AHOLD	42	O	**Address Hold Request**. This is the address hold request signal to processor.
EADSJ	43	O	**External Address Strobe**. This signal indicates that a valid external address has been driven onto the CPU address pins to be used for cache snooping cycle.
KENOJ	44	O	**Cache Enable Output**. This is the cache enable signal to CPU.
RSTDRV	131	I	**Chip Initiation**. This signal is used to initialize the M1489 chip internal state machines and registers.
CPUCLK1	129	I	**CPU bus Clock**

M1489 Pin Description Table (continued)

Name	Number	Type	Description
Memory Control			
RASJ[3:0]	68~71	O	**Low Address Strobe**. These are the memory module row address strobe signals. The RASJ0 applies to bank 0 memory module and RASJ1 applies to bank 1, RASJ2 applies to bank2, and the RASJ3 applies to bank3.
CASJ[3:0]	63~66	O	**Column Address Strobe**. These are the memory module column address strobe signals. The CASJ0 applies to byte 0, CASJ1 applies to byte 1, CASJ2 applies to byte 2, and CASJ3 applies to byte 3.
MA[11:0]	49-51, 54-62	I/O	**Memory Address**. These are the memory address signals. These signals will change to PWCNTL0-PWCNTL11(power control signals) during the power-control output cycle. These pins will be input polarity during the power-on reset period for initializing the power-control default value of the internal ports.
MWEJ	67	I/O	**Memory Write Enable**. This is the memory write enable signal.
L2 Cache Controller interface			
COEJ[1:0]	194, 201	O	**Cache Output Enable**. These are the cache output enable signals with which the single chip can control the external 2 bank cache system. The COEJ0 applies to the bank 0 cache and COEJ1 applies to the bank 1.
CWEJ [1:0]	196, 200	O	**Cache Write Enable**. These are the cache write enable signals. The CWEJ0 applies to bank 0 cache and the CWEJ1 applies to bank 1 cache.
CCSJ[3:0] /PD[3:0]	202, 198, 195, 193	I/O	**Cache Chip Select**. These are the cache system chip select signals. These pins can also be used as DRAM parity data bytes [3:0] through hardware configuration.
TAGWEJ	4	O	**Tag Write Enable**. This is the tag RAM write enable signal.
TAG[7:0]	203~207, 1~3	I/O	**Tag Data**. These are the cache tag data bits.
A3I	199	O	**Cache Address 3**. This is the cache address line 3 for bank 0 cache.
A3II	197	O	**Cache Address 3**. This is the cache address line 3 for bank 1 cache.
SMM Signal			
SMIACTJ	192	I	**System Management Interrupt Active**. This signal is an active low input indicating that the processor is operating at SMM.
Linkbus Interface			
CLEAROKJ	153	B	**CMP(M1489) Internal Buffers Cleared OK**. This signal is used to indicate the CMP internal buffers usage status and the PCI slave devices respondent action.
CMPGNTJ	154	I	**CMP Grant signal**. It indicates to the CMP/CPU that access to the system resource and bus ownership has been granted.
CMPSTJ	152	B	**CMP Status Ready**. This signal is used to indicate the CMP's status or data has been ready and valid on the link-bus.
IBCSTJ	155	I	**IBC Status Ready**. This signal is used to indicate the IBC's status or data has been ready and valid on the link-bus.

M1489 Pin Description Table (continued)

Name	Number	Type	Description
IDE Interface			
HDD[15:0]	85~101	B	**Disk Data[15:0]**. These are the 16-bit data bus which connects to the IDE drives. HDD[7:0] define the lowest data byte while HDD[15:8] define the most significant data byte. The HDD bus is normally in a high-impedance state and is driven by the M1489 only during the HDIOWJ command pulse.
HDIOWJ	84	O	**Disk I/O Write Command**. This is an active low output which enables data to be written to the IDE drive.
HDIORJ	83	O	**Disk I/O Read Command**. This is an active low output which enables data to be read from the IDE drive.
HDIORDYJ	82	I	**Disk Ready**. This is an input which is sampled at the clock rising edge at the programmed end of the command cycle. If HDIORDYJ is sampled high, the command is terminated. If it is sampled low the command cycle is extended. HDIORDYJ will be sampled with every positive CLK edge until it is tested high. Once sampled high, the command will end normally. Note that an external 1K-Ohm pull-up resistor is recommended for this signal.
HDIO16J	81	I	**Disk Chip Select 16**. This is an active-low input which indicates that the disk drive is ready to perform a 16-bit data transfer. The signal connects directly to the ATA connector and is typically driven active during IDE controller transfers to the drive's 1F0h data port. Note that an external 1K-Ohm pull-up resister is recommended for this signal.
HDA[2:0]	79, 80 77	O	**Disk Address[2:0]**. These are normally outputs to the ATA connector for register selection in the drives. These signals are decoded from the GA[2] and BEJ[3:0] inputs.
HDCSJ[3:0]	75,76 73,74	O	**Disk Chip Select**. These are active low outputs which are used to select control/command block registers in the drives.
PCI Interface			
PAD[31:0]	102~151	I/O	**Address and Data Multiplexed pins**. During the first clock of a PCI transaction PAD[31:0] contain a physical address(32 bits). During subsequent clocks PAD[31:0] contain data.
PAR	114	I/O	**Parity bit**. Parity is even parity across AD[31:00] and CBE#[3:0]. The M1489 generates parity bit (1)when it acts as a PCI slave in PCI master read cycle data phase, or (2)when it acts as a PCI master in CPU write cycle address and data phase, or (3)when it acts as a PCI master in CPU read cycle address phase.
CBEJ[3:0]	147,141, 137,123	I/O	**Byte Enables**. These signals indicate active bytes during read and write cycle. These pins are outputs when PCI master cycle. Otherwise, these pins are inputs.
FRAMEJ	111	I/O	**Cycle Frame**. It indicates the beginning and duration of a PCI access. This pin is output when M1489 acts as a PCI master. This pin is input when M1489 acts as a PCI slave.
TRDYJ	112	I/O	**Target Ready**. It indicates the target's (selected device's) ability to complete the current data phase of the transaction. TRDYJ is used in conjunction with IRDYJ. This pin is output when M1489 acts as a slave, and input when M1489 acts as a master.
STOPJ	113	I/O	**Stop**. It indicates the current Target is requesting the Master to stop the current transaction. This pin is output in PCI master cycle when multiple data transfer is disabled, and input when PCI slave requests to stop current cycle.
PCICLK	127	I	**PCI system Clock**

M1489 Pin Description Table (continued)

Name	Number	Type	Description
PCI Interface			
DEVSELJ	139	I/O	**Device select**. It indicates the target device has decoded the address as its own cycle. This pin is output when M1489 acts as a PCI slave, and input when M1489 acts as a PCI master.
IRDYJ	140	I/O	**Initiator Ready**. It indicates the PCI bus master's ability to complete the current data phase of the transaction. This pin is output when M1489 acts as a PCI master, and input when M1489 acts as a PCI slave.
PERRJ	138	I/O	**Parity Error**. It may be pulsed by any selected device which detects a data parity error. M1489 combines SERRJ and PERRJ to create error event to M1487 to generate NMI.
Power			
Vcc[1], Vcc[6]	22,182	(3/5V)	System 5V power supply signals for 5V/5V- tolerance CPU system. Or, system 3.3V power supply signals for pure 3.3V interface CPU system.
Vcc[2:5]	52,78, 130,144		System 5V power supply signals.
GND[1:9]	34, 53, 72, 90, 104, 128,156, 168,208		System Ground level signals.

Table 2-2. M1487 Pin Description Table

Name	Number	Type	Description
Clock & reset interface			
CPUCLK	61	I	**CPU bus Clock**
PCICLK	46	I	**PCI bus Clock**
OSC	49	I	**14.318MHz Input**. This is a clock input signal.
ATCLK	70	O	**System Clock Output**. This is AT clock output signal. This clock can be set to CPUCLK divided by 3,4,5,6,8 or 7.16 MHz.
PWG	13	I	**Power Good**. This input signal is a Schmitt trigger pad signal. It comes from the power supply to indicate that power is available and stable.
CPURST	20	O	**CPU Reset**. This signal resets the CPU processor.
SYSRST	63	O	**Cold Reset**. System cold reset.
SYSRSTJ	81	O	**Cold Reset**. The signal is the inversed cold reset.
CPU interface			
A20MJ	22	O	**Address 20 Mask**. This is the Address line 20 mask signal.
INTR	23	O	**Interrupt Request**. This is the interrupt signal generated by the internal 8259. It is synchronized with CPUCLK.
FERRJ	16	I	**Floating Point Error**.
IGNNEJ	17	B	**Ignore Numeric Error**.
NMI	18	O	**Non-Maskable Interrupt**. This is the non-maskable interrupt request signal.
SMIJ	19	B	**System Management Interrupt**. This signal invokes the System Management Mode(SMM).
STPCLKJ	21	O	**Stop Clock Request**. This signal indicates that a request to Intel processor has been made to turn off its CLK input.
ISA bus interface			
IO16J	110	I	**External 16-Bit I/O Chip Select**. This is the 16-bit I/O devices select indicating signal.
MEM16J	111	B	**External 16-Bit Memory Chip Select**. This is the 16 bit memory devices select indicating signal.
ZMRJ	67	B	**Memory Read**. This signal is an input in master cycle but an output in other cycles. In CPU ISA cycles, this signal is driven by chip internal control circuits. In DMA cycles, this signal is driven by the internal DMA controllers. In refresh cycles, this signal is driven by the internal refresh circuits. In master cycles, this signal is driven by external master devices.
ZMWJ	79	B	**Memory Write**. This signal is an input in master cycle but an output in other cycles. In CPU ISA cycles, this signal is driven by chip internal control circuits. In DMA cycles, this signal is driven by the internal DMA controllers. In master cycles, this signal is driven by external master devices.
ZSMEMRJ	66	O	**System Memory Read**. This is a tri-state output signal. It is driven low only when the system executes a below 1 Mbyte ISA memory read cycle. Otherwise, it is a tri-state status.
ZSMEMWJ	76	O	**System Memory Write**. This is a tri-state output signal. It is driven low only when the system executes a below 1 Mbyte ISA memory write cycle. Otherwise, it is a tri-state status.

M1487 Pin Description Table (continued)

Name	Number	Type	Description
ISA bus interface			
IOCHRDYJ	139	B	**I/O Channel Ready**. This input signal is used to extend the ISA command width for the CPU and DMA cycles. In memory access events, this signal is output polarity pending the ISA MST/DMA cycle until the linkbus system finishes the data transferred access.
N0WSJ	2	I	**ISA Bus Zero-Wait State**. This is the ISA device zero-wait state indicator signal. This signal terminates the CPU ISA command immediately.
ZBALE	68	O	**Buffer Address Latch Enable**. This is the buffered address latch enable signal. A high pulse with half ATCLK is generated at the beginning of CPU ISA cycle for the external devices to latch the system address. During the CPU bus releasing to ISA system cycle, this signal is kept at a high level status.
IORJ	69	B	**I/O Read**. This signal is an input in master cycle but is output in other cycles. In CPU ISA cycles, this signal is driven by chip internal control circuits. In DMA cycles, this signal is driven by the internal DMA controllers. In master cycles, this signal is driven by the external master devices.
IOWJ	77	B	**I/O Write**. This signal is an input in master cycle but is output in other cycles. In CPU ISA cycles, this signal is driven by chip internal control circuits. In DMA cycles, this signal is driven by the internal DMA controllers. In master cycles, this signal is driven by the external master devices.
MASTERJ	82	I	**Master**. This is ISA master access indicating signal.
ZAEN	140	O	**Address Enable**. This is the address enable signal. In CPU or master cycle, this signal is driven low to enable the external devices to decode the I/O address. In other cycles, this signal is driven high to inhibit I/O address decoding.
SBHEJ	159	B	**Slot Byte High Enable**. This is the system byte high enable signal. In CPU cycle, this signal is generated by BE3J-BE0J and the chip internal control circuit. In DMA cycle, it is generated by internal 8237. In refresh cycle, it is generated by the internal refresh circuits. In master cycle, it is an input polarity signal and is driven by the master device.
LA[23:17]	112~118	B	**Latch Address[23:17]**. These addresses are connected to slot address. They are input during ISA MASTER cycle.
SA[19:17]	141~143	B	**Slot Address[19:17]**. These addresses are connected to slot address. They are tri-state during ISA MASTER cycle and driven low as refresh cycle.
SA[16:2]	145~157, 8,9	B	**Slot Address[16:2]**. These addresses are connected to slot addresses. They are input for ISA MASTER cycle and driven output for CPU, DMA, PCI MASTER and REFRESH cycles.
SA[1]	4	B	**Slot Address 1**. This is the system address line 1 signal. In CPU cycle, this signal is generated by BE3J-BE0J and the chip internal control circuit. In DMA cycle, it is generated by the internal 8237. In refresh cycle, it is generated by the internal refresh circuits. In master cycle, it is an input polarity signal and is driven by the master device.
SA[0]	7	B	**Slot Address 0**. This is the system address line 0 signal. In CPU cycle, this signal is generated by BE3J-BE0J and the chip internal control circuit. In DMA cycle, it is generated by the internal 8237. In refresh cycle, it is generated by the internal refresh circuits. In master cycle, it is an input polarity signal and is driven by the master device.

M1487 Pin Description Table (continued)

Name	Number	Type	Description
ISA bus interface			
SD[15:0]	119, 121~127, 130~137	B	**Slot Data Bus**. These are the system data lines.
REFRESHJ	158	B	**Refresh**. The signal is input polarity at master cycle, but it is output pin at other cycles.
IOCHCKJ	129	I	**I/O Channel Check**. This connects to I/O slot channel check.
DRQ[7:5], DRQ[3:0]	109,107, 105,89, 91,87,103	I	**DMA Request Input**. This are the DMA request input signals.
DACKJ [7:5], DACKJ [3:0]	108,106, 104,84, 94,86,102	O	**DMA Acknowledge Output**. These are DACK demultiplex select signals.
TC	95	B	**Terminal Count**. This is the DMA channel terminal count indicating signal.
IRQ[15:14] IRQ[12:9], IRQ[7:3],	99~101, 97, 96, 83, 88~90, 92	B	**Interrupt Request Input**. This is the Interrupt request input signal.
IRQ[1]	11	I	When internal KBC be enabled, this pin will be changed to keyboard inhibit pin.
IRQ8J	3	I	
PCI bus interface			
PREQJ [2:0]	54,53,50	I	**PCI Request signal**. They indicate to the internal arbiter that the corresponding PCI device desires to use the bus. M1489/M1487 supports up to 3 PCI bus masters.
PGNTJ [2:0]	55,51,52	O	**PCI Grant signals**. They indicate to the requesting device that access to the bus has been granted.
FRAMEJ	47	I	**Cycle Frame**. This signal indicates the beginning and duration of a PCI access.
IRDYJ	48	I	**Initiator Ready**. This signal indicates the PCI bus master's ability to complete the current data phase of the transaction.
INTJ[3:0]	56~59	I	**Interrupt Request inputs**. These pins come from PCI slots. They are Level_triggered and active low. They are translated to be edge_triggered, then connected to system interrupt controller.
Peripheral interface			
XBUSCSJ	73	B	**X-Bus Chip Select**. This X-Bus chip select indicating signal includes ROM and keyboard.
RTCAS	78	O	**RTC Address Strobe**. This is the RTC address strobe signal.
OSC1, OSC2	14,15	I	**Oscillator**. These pins are the crystal inputs and provide for an external 32.768KHz quartz crystal. In the absence of a crystal, an oscillator output of 32.768KHz maybe fed into OSC1 input.
SPEAK	65	O	**Speaker Data**. This is the speaker data.
TURBO	64	I	**System speed**. This is connected to the TURBO switch to detect hardware setting system speed.
EXTSMI	74	I	**External Switch**. This switch is caused to assert SMIJ for power saving or to wake up the system through the SMI routine.
CPUSPD	75	O	**CPU Speed**. This is speed LED indicating signal.
CLKCTR	72	O	**Clock Generator Powerdown Control**. When it is logic high, the system will be in high performance operation. When it is logic low, the system will do deturbo or power-down operation.
ENRTC/ RTCSJ	71	B	**Enable Internal RTC Indicator**. When this pin is pulled-up during the cold reset period, the internal RTC will be enabled. When this pin is pulled-down during the cold reset period, the internal RTC will be disabled and this pin function will be changed to RTC chip select.

M1487 Pin Description Table (continued)

Name	Number	Type	Description
Link bus interface			
CLEAROKJ	44	I	**CMP(M1489) Internal Buffers Cleared OK**. This signal is used to indicate M1489's internal buffers usage status and the PCI slave devices respondent action.
CMPGNTJ	43	O	**CMP Grant signal**. It indicates to the CMP/CPU that access to the system resource and bus ownership has been granted.
CMPSTJ	45	I	**CMP Status Ready**. This signal is used to indicate the CMP's status or data has been ready and valid on the link-bus.
IBCSTJ	42	B	**IBC Status Ready**. This signal is used to indicate the IBC's status or data has been ready and valid on the link-bus.
GA[17:2]	24~39	B	**Linkbus Data**. These signals are used to transfer the status, command, system address, and system data between M1489 and M1487.
Keyboard Controller			
KBCLK	5	B	**Keyboard Clock**
KBDATA	6	B	**Keyboard Data**
Power			
Vcc[5:1]	1,60, 80, 120, 144	P	System 5V power supply signals.
GND[7:1]	10, 41, 62, 98, 128, 138,160	P	System Ground level signals.
VRTC_BAT	12	P	This power pin should be connected to the RTC battery supplier when the internal RTC is enabled.
Vcc_3/5V	40	P	System 5V power supply signals for 5V/5V- tolerance CPU system. Or, system 3.3V power supply signals for pure 3.3V interface CPU system.

2.3 M1489 Numerical Pin List

Number	Type	Name
1	B	TAG5
2	B	TAG4
3	B	TAG3
4	O	TAGWEJ
5	B	GD0
6	B	GD1
7	B	GD2
8	B	GD3
9	B	GD4
10	B	GD5
11	B	GD6
12	B	GD7
13	B	GD8
14	B	GD9
15	B	GD10
16	B	GD11
17	B	GD12
18	B	GD13
19	B	GD14
20	B	GD15
21	B	GD16
22	P	Vcc1
23	B	GD17
24	B	GD18
25	B	GD19
26	B	GD20
27	B	GD21
28	B	GD22
29	B	GD23
30	B	GD24
31	B	GD25
32	B	GD26
33	B	GD27
34	P	GND1
35	B	GD28
36	B	GD29
37	B	GD30
38	B	GD31
39	O	RDYOJ
40	O	BRDYJ
41	O	BOFFJ
42	O	AHOLD
43	O	EADSJ
44	O	KENOJ
45	B	BEJ3

Number	Type	Name
46	B	BEJ1
47	B	BEJ0
48	B	BEJ2
49	B	MA7
50	B	MA6
51	B	MA5
52	P	Vcc2
53	P	GND2
54	B	MA4
55	B	MA3
56	B	MA2
57	B	MA1
58	B	MA0
59	O	MA11
60	O	MA10
61	O	MA9
62	O	MA8
63	O	CASJ3
64	O	CASJ2
65	O	CASJ1
66	O	CASJ0
67	B	WEJ
68	O	RAS3
69	O	RAS2
70	O	RAS1
71	O	RAS0
72	P	GND3
73	O	HDCSJ1
74	O	HDCSJ0
75	O	HDCSJ3
76	O	HDCSJ2
77	O	HDA0
78	P	Vcc3
79	O	HDA2
80	O	HDA1
81	I	HDIO16J
82	I	HDIORDY
83	O	HDIORJ
84	O	HDIOWJ
85	B	HDD15
86	B	HDD14
87	B	HDD0
88	B	HDD13
89	B	HDD1
90	P	GND4

M1489 Numerical Pin List (continued)

Number	Type	Name
91	B	HDD12
92	B	HDD2
93	B	HDD11
94	B	HDD3
95	B	HDD10
96	B	HDD4
97	B	HDD9
98	B	HDD5
99	B	HDD8
100	B	HDD6
101	B	HDD7
102	B	PAD30
103	B	PAD28
104	P	GND4
105	B	PAD26
106	B	PAD24
107	B	PAD22
108	B	PAD20
109	B	PAD18
110	B	PAD16
111	B	FRAMEJ
112	B	TRDYJ
113	B	STOPJ
114	B	PAR
115	B	PAD15
116	B	PAD13
117	B	PAD11
118	B	PAD9
119	B	PAD4
120	B	PAD2
121	B	PAD6
122	B	PAD0
123	B	CBEJ0
124	B	PAD7
125	B	PAD5
126	B	PAD8
127	B	PCICLK
128	B	GND6
129	B	CPUCLK1
130	B	Vcc4
131	B	RSTDRV
132	B	PAD1
133	B	PAD3
134	B	PAD10
135	B	PAD12

Number	Type	Name
136	B	PAD14
137	B	CBEJ1
138	B	PERRJ
139	B	DEVSELJ
140	B	IRDYJ
141	B	CBEJ2
142	B	PAD17
143	B	PAD19
144	P	Vcc5
145	B	PAD21
146	B	PAD23
147	B	CBEJ3
148	B	PAD25
149	B	PAD27
150	B	PAD29
151	B	PAD31
152	B	CMPSTJ
153	B	CLEAROKJ
154	I	CMPGNTJ
155	I	IBCSTJ
156	P	GND7
157	B	GA2
158	B	GA3
159	B	GA17
160	B	GA16
161	B	GA15
162	B	GA11
163	B	GA10
164	B	GA12
165	B	GA9
166	P	GA14
167	B	GA8
168	P	GND8
169	B	GA13
170	B	GA7
171	B	GA6
172	B	GA5
173	B	GA4
174	B	GA18
175	B	GA19
176	B	GA20
177	B	GA21
178	B	GA22
179	B	GA23
180	B	GA24

M1489 Numerical Pin List (continued)

Number	Type	Name
181	B	GA31
182	P	Vcc6
183	B	GA25
184	B	GA26
185	I	LOCKJ
186	B	ADSJ
187	B	MIOJ
188	B	DCJ
189	B	WRJ
190	B	PCD
191	I	HITMJ
192	I	SMIACKJ
193	B	CCSJ0
194	O	COEJ1
195	B	CCSJ1
196	O	CWEJ1
197	O	CA2
198	B	CCSJ2
199	O	CA3
200	O	CWEJ0
201	O	COEJ0
202	B	CCSJ3
203	B	TAG0
204	B	TAG1
205	B	TAG2
206	B	TAG7
207	B	TAG6
208	P	GND9

2.4 M1489 Alphabetical Pin List

Number	Type	Name
186	B	ADSJ
42	O	AHOLD
47	B	BEJ0
46	B	BEJ1
48	B	BEJ2
45	B	BEJ3
41	O	BOFFJ
40	O	BRDYJ
197	O	CA2
199	O	CA3
63	O	CASJ3
64	O	CASJ2
65	O	CASJ1
66	O	CASJ0
123	B	CBEJ0
137	B	CBEJ1
141	B	CBEJ2
147	B	CBEJ3
193	B	CCSJ0
195	B	CCSJ1
198	B	CCSJ2
202	B	CCSJ3
153	B	CLEAROKJ
154	I	CMPGNTJ
152	B	CMPSTJ
201	O	COEJ0
194	O	COEJ1
129	B	CPUCLK1
200	O	CWEJ0
196	O	CWEJ1
188	B	DCJ
139	B	DEVSELJ
43	O	EADSJ
111	B	FRAMEJ
157	B	GA2
158	B	GA3
173	B	GA4
172	B	GA5
171	B	GA6
170	B	GA7
167	B	GA8
165	B	GA9
163	B	GA10
162	B	GA11
164	B	GA12

M1489 Alphabetical Pin List (continued)

Number	Type	Name
169	B	GA13
166	P	GA14
161	B	GA15
160	B	GA16
159	B	GA17
174	B	GA18
175	B	GA19
176	B	GA20
177	B	GA21
178	B	GA22
179	B	GA23
180	B	GA24
183	B	GA25
184	B	GA26
181	B	GA31
5	B	GD0
6	B	GD1
7	B	GD2
8	B	GD3
9	B	GD4
10	B	GD5
11	B	GD6
12	B	GD7
13	B	GD8
14	B	GD9
15	B	GD10
16	B	GD11
17	B	GD12
18	B	GD13
19	B	GD14
20	B	GD15
21	B	GD16
23	B	GD17
24	B	GD18
25	B	GD19
26	B	GD20
27	B	GD21
28	B	GD22
29	B	GD23
30	B	GD24
31	B	GD25
32	B	GD26
33	B	GD27
35	B	GD28
36	B	GD29

Number	Type	Name
37	B	GD30
38	B	GD31
34	P	GND1
53	P	GND2
72	P	GND3
90	P	GND4
104	P	GND5
128	B	GND6
156	P	GND7
168	P	GND8
208	P	GND9
77	O	HDA0
80	O	HDA1
79	O	HDA2
74	O	HDCSJ0
73	O	HDCSJ1
76	O	HDCSJ2
75	O	HDCSJ3
87	B	HDD0
89	B	HDD1
92	B	HDD2
94	B	HDD3
96	B	HDD4
98	B	HDD5
100	B	HDD6
101	B	HDD7
99	B	HDD8
97	B	HDD9
95	B	HDD10
93	B	HDD11
91	B	HDD12
88	B	HDD13
86	B	HDD14
85	B	HDD15
81	I	HDIO16J
82	I	HDIORDY
83	O	HDIORJ
84	O	HDIOWJ
191	I	HITMJ
140	B	IRDYJ
155	I	IBCSTJ
44	O	KENOJ
185	I	LOCKJ
58	B	MA0
57	B	MA1

M1489 Alphabetical Pin List (continued)

Number	Type	Name
56	B	MA2
55	B	MA3
54	B	MA4
51	B	MA5
50	B	MA6
49	B	MA7
62	O	MA8
61	O	MA9
60	O	MA10
59	O	MA11
187	B	MIOJ
122	B	PAD0
132	B	PAD1
120	B	PAD2
133	B	PAD3
119	B	PAD4
125	B	PAD5
121	B	PAD6
124	B	PAD7
126	B	PAD8
118	B	PAD9
134	B	PAD10
117	B	PAD11
135	B	PAD12
116	B	PAD13
136	B	PAD14
115	B	PAD15
110	B	PAD16
142	B	PAD17
109	B	PAD18
143	B	PAD19
108	B	PAD20
145	B	PAD21
107	B	PAD22
146	B	PAD23
106	B	PAD24
148	B	PAD25
105	B	PAD26
149	B	PAD27
103	B	PAD28
150	B	PAD29
102	B	PAD30
151	B	PAD31
114	B	PAR
190	B	PCD

Number	Type	Name
127	B	PCICLK
138	B	PERRJ
71	O	RAS0
70	O	RAS1
69	O	RAS2
68	O	RAS3
39	O	RDYOJ
131	B	RSTDRV
192	I	SMIACKJ
113	B	STOPJ
203	B	TAG0
204	B	TAG1
205	B	TAG2
3	B	TAG3
2	B	TAG4
1	B	TAG5
207	B	TAG6
206	B	TAG7
4	O	TAGWEJ
112	B	TRDYJ
22	P	Vcc1
52	P	Vcc2
78	P	Vcc3
130	B	Vcc4
144	P	Vcc5
182	P	Vcc6
67	B	WEJ
189	B	WRJ

2.5 M1487 Numerical Pin List

Number	Type	Name
1	P	Vcc5
2	I	N0WSJ
3	I	IRQ8J
4	B	SA1
5	B	KBCLK
6	B	KBDATA
7	B	SA0
8	B	SA14
9	B	SA13
10	P	GND7
11	I	IRQ1
12	P	VBAT
13	I	PWG
14	I	OSC1
15	I	OSC2
16	I	FERRJ
17	B	IGNNEJ
18	O	NMI
19	B	SMIJ
20	O	CPURST
21	O	STPCLKJ
22	O	A20MJ
23	O	INTR
24	B	GA4
25	B	GA5
26	B	GA6
27	B	GA7
28	B	GA13
29	B	GA8
30	B	GA14
31	B	GA9
32	B	GA12
33	B	GA10
34	B	GA11
35	B	GA15
36	B	GA16
37	B	GA17
38	B	GA3
39	B	GA2
40	P	Vcc6

Number	Type	Name
41	P	GND1
42	I	IBCSTJ
43	O	CMPGNTJ
44	O	CLEAROKJ
45	B	CMPSTJ
46	I	PCICLK
47	I	FRAMEJ
48	I	IRDYJ
49	I	OSC
50	I	PREQJ0
51	O	PGNTJ1
52	O	PGNTJ0
53	I	PREQJ1
54	I	PREQJ2
55	O	PGNTJ2
56	I	INT2J
57	I	INT0J
58	I	INT3J
59	I	INT1J
60	P	Vcc1
61	I	CPUCLK
62	P	GND2
63	O	SYSRST
64	I	TURBO
65	O	SPEAK
66	O	ZSMEMRJ
67	B	ZMRJ
68	O	ZBALE
69	B	IORJ
70	O	ATCLK
71	B	ENRTC
72	O	CLKCTR
73	B	XBUSCSJ
74	I	EXTSMI
75	O	CPUSPD
76	O	ZSMEMWJ
77	B	IOWJ
78	O	RTCAS
79	B	ZMWJ
80	P	Vcc2

M1487 Numerical Pin List (continued)

Number	Type	Name
81	O	SYSRSTJ
82	I	MASTERJ
83	B	IRQ9
84	O	DACK3
85	I	DRQ3
86	O	DACK1
87	I	DRQ1
88	B	IRQ7
89	B	IRQ6
90	B	IRQ5
91	O	DRQ2
92	B	IRQ4
93	B	IRQ3
94	O	DACK2
95	B	TC
96	B	IRQ10
97	B	IRQ11
98	P	GND3
99	B	IRQ12
100	B	IRQ15
101	B	IRQ14
102	O	DACK0
103	I	DRQ0
104	O	DACK5
105	I	DRQ5
106	O	DACK6
107	I	DRQ6
108	O	DACK7
109	I	DRQ7
110	I	IO16J
111	B	MEM16J
112	B	LA23
113	B	LA22
114	B	LA21
115	B	LA20
116	B	LA19
117	B	LA18
118	B	LA17
119	B	SD8
120	P	Vcc3

Number	Type	Name
121	B	SD9
122	B	SD15
123	B	SD14
124	B	SD13
125	B	SD12
126	B	SD11
127	B	SD10
128	P	GND4
129	I	IOCHKJ
130	B	SD7
131	B	SD6
132	B	SD5
133	B	SD4
134	B	SD3
135	B	SD2
136	B	SD1
137	B	SD0
138	P	GND5
139	B	IOCHRDYJ
140	O	ZAEN
141	B	SA19
142	B	SA18
143	B	SA17
144	P	Vcc4
145	B	SA16
146	B	SA12
147	B	SA11
148	B	SA10
149	B	SA9
150	B	SA8
151	B	SA7
152	B	SA6
153	B	SA15
154	B	SA5
155	B	SA4
156	B	SA3
157	B	SA2
158	B	REFSHJ
159	B	SBHEJ
160	P	GND6

2.6 M1487 Alphabetical Pin List

Number	Type	Name
22	O	A20MJ
70	O	ATCLK
72	O	CLKCTR
44	O	CLEAROKJ
43	O	CMPGNTJ
45	B	CMPSTJ
61	I	CPUCLK
20	O	CPURST
75	O	CPUSPD
102	O	DACK0
86	O	DACK1
94	O	DACK2
84	O	DACK3
104	O	DACK5
106	O	DACK6
108	O	DACK7
103	I	DRQ0
87	I	DRQ1
91	O	DRQ2
85	I	DRQ3
105	I	DRQ5
107	I	DRQ6
109	I	DRQ7
71	B	ENRTC
74	I	EXTSMI
16	I	FERRJ
47	I	FRAMEJ
39	B	GA2
38	B	GA3
24	B	GA4
25	B	GA5
26	B	GA6
27	B	GA7
29	B	GA8
31	B	GA9
33	B	GA10
34	B	GA11
32	B	GA12
28	B	GA13
30	B	GA14

Number	Type	Name
35	B	GA15
36	B	GA16
37	B	GA17
41	P	GND1
62	P	GND2
98	P	GND3
128	P	GND4
138	P	GND5
160	P	GND6
10	P	GND7
42	I	IBCSTJ
56	I	INT2J
57	I	INT0J
58	I	INT3J
59	I	INT1J
17	B	IGNNEJ
23	O	INTR
139	B	IOCHRDYJ
69	B	IORJ
77	B	IOWJ
110	I	IO16J
129	I	IOCHKJ
48	I	IRDYJ
11	I	IRQ1
93	B	IRQ3
92	B	IRQ4
90	B	IRQ5
89	B	IRQ6
88	B	IRQ7
3	I	IRQ8J
83	B	IRQ9
96	B	IRQ10
97	B	IRQ11
99	B	IRQ12
101	B	IRQ14
100	B	IRQ15
5	B	KBCLK
6	B	KBDATA
118	B	LA17
117	B	LA18

M1487 Alphabetical Pin List

Number	Type	Name
116	B	LA19
115	B	LA20
114	B	LA21
113	B	LA22
112	B	LA23
82	I	MASTERJ
111	B	MEM16J
18	O	NMI
2	I	N0WSJ
14	I	OSC1
15	I	OSC2
49	I	OSC
46	I	PCICLK
52	O	PGNTJ0
51	O	PGNTJ1
55	O	PGNTJ2
50	I	PREQJ0
53	I	PREQJ1
54	I	PREQJ2
13	I	PWG
158	B	REFSHJ
78	O	RTCAS
7	B	SA0
4	B	SA1
157	B	SA2
156	B	SA3
155	B	SA4
154	B	SA5
152	B	SA6
151	B	SA7
150	B	SA8
149	B	SA9
148	B	SA10
147	B	SA11
146	B	SA12
9	B	SA13
8	B	SA14
153	B	SA15
145	B	SA16
143	B	SA17

Number	Type	Name
142	B	SA18
141	B	SA19
159	B	SBHEJ
137	B	SD0
136	B	SD1
135	B	SD2
134	B	SD3
133	B	SD4
132	B	SD5
131	B	SD6
130	B	SD7
119	B	SD8
121	B	SD9
127	B	SD10
126	B	SD11
125	B	SD12
124	B	SD13
123	B	SD14
122	B	SD15
19	B	SMIJ
65	O	SPEAK
21	O	STPCLKJ
63	O	SYSRST
81	O	SYSRSTJ
95	B	TC
64	I	TURBO
12	P	VBAT
60	P	Vcc1
80	P	Vcc2
120	P	Vcc3
144	P	Vcc4
1	P	Vcc5
40	P	Vcc6
73	B	XBUSCSJ
140	O	ZAEN
68	O	ZBALE
67	B	ZMRJ
79	B	ZMWJ
66	O	ZSMEMRJ
76	O	ZSMEMWJ

2.7 Hardware Setup

Hardware Setup Table of M1489/M1487

M1489 (CMP) Chip Hardware Setup Table

Pin No.	Pin Name	Setup	Configuration
152	CMPSTJ	Pull-up/Pull-down	PCICLK = CPUCLK/ PCICLK = 1/2 CPUCLK
153	CLEAROKJ	Pull-up/Pull-down	L2 CSJ / DRAM Parity
138	PCIPERRJ	Pull-up/Pull-down	PCI PERRJ/MEM buffer DIR
67	MWEJ	Pull-up/Pull-down	5V / 3.3V CPU interface

M1487 (IBC) Chip Hardware Setup Table

Pin No.	Pin Name	Setup	Configuration
73	XBUSCSJ	Pull-up/Pull-down	8/16 bits ROM select
71	ENRTC	Pull-up/Pull-down	EN/DISable int. RTC
42	IBCSTJ	Pull-up/Pull-down	EN/DISable int. KBC
45	CMPSTJ	Pull-up/Pull-down	PCICLK = CPUCLK/ PCICLK = 1/2 CPUCLK
43	CMPGNTJ	Pull-up/Pull-down	5V / 3.3V CPU interface
17	IGNNEJ	Pull-up/Pull-down	Normal/Test mode setting

2.8 M1489/M1487 Hardware Reference Manual

1. Clock signal connection:

(1) Clock signal connection:

(a) The clock design philosophy of M1489 uses CPUCLK1(pin 129) as the clock base of internal state machine and uses PCICLK (pin 127) as the phase reference in 2X architecture (when CPUCLK1 > 33 MHz). While in 1X architecture (when CPUCLK1 £ 33 MHz), PCICLK is ignored internally. The relation between CPUCLK1 and PCICLK is not so concerned with M1489, which means CPUCLK1 can lead PCICLK or lag PCICLK. But for the setup and hold time issue, M1489 prefers these two clocks not to have skew.

The clock design philosophy of M1487 uses CPUCLK (pin 87) as the clock base of internal state machine and uses PCICLK (pin 46) as the phase reference in 2X architecture (when CPUCLK > 33 MHz). While in 1X architecture (when CPUCLK £ 33 MHz), PCICLK is ignored internally. The relation between CPUCLK and PCICLK is not so concerned with M1487, that means CPUCLK can lead PCICLK or lag PCICLK. But for the setup and hold time issue, M1487 prefers these two clocks not to have skew.

(b) If the system uses the 2X architecture, the CPUCLK1 (pin 129) of M1489 and the CPUCLK (pin 61) of M1487 should be sourced by 2x clock source and the PCICLK (pin 127) of M1489 and the PCICLK (pin 46) of M1487 is sourced by 1x clock source.

(c) If the system uses the 1X architecture, the CPUCLK1 (pin 129) of M1489 and the CPUCLK (pin 61) of M1487 should be sourced by 1x clock source. While the PCICLK (pin 127) of M1489 and the PCICLK (pin 46) of M1487 is sourced by 1x clock source but ignored internally.

(2) 2X system:

CMPSTJ (pin 152 of M1489): pull low

The M1489 internal state machines are driven by the CPUCLK1 (pin 129) and phase is recognized by the PCICLK (pin 127).

The M1487 internal state machines are driven by the CPUCLK (pin 61) and phase is recognized by the PCICLK (pin 46).

(3) 1X system:

CMPSTJ (pin 152 of M1489): pull high

The M1489 internal state machines are driven by the CPUCLK1 (pin 129) and does not need phase recognition.

The M1487 internal state machines are driven by the CPUCLK (pin 61) and does not need phase recognition.

2. CCSJ[3:0]/PD[3:0] signals connection:

(a) CLEAROKJ(pin 153) of M1489 : pull high
M1489 pins 202, 198, 195, 193 are used as CCSJ[3:0] for 2nd level data cache chip select. In this configuration, DRAM parity is not supported by M1489.

(b) CLEAROKJ (pin 153) of M1489: pull low
M1489 pins 202, 198, 195, 193 are used as PD[3:0] for DRAM parity data. In this configuration, motherboard needs a 74F08 to decode CCSJ[3:0] for 2nd level data cache chip select using CPU command WRJ AND with BEJ[3:0]. PD[3:0] is connected to DRAM parity data lines directly, but cannot be connected to CPU parity data lines. This must be guaranteed to prevent parity data conflict. M1489 will do the parity check when reading DRAM data, and generate parity data to DRAM when writing DRAM data. When DRAM parity error is detected, an NMI will be issued to CPU.

3. PERRJ/MDIR signal select:

(a) Pin 138 of M1489: pull high
M1489 pin 138 is used as PCI PERRJ. In this configuration, PCI parity check is supported.

(b) Pin 138 of M1489: pull low
M1489 pin 138 is used as MDIR. MDIR is the memory data buffer direction to isolate CPU data bus GD[31:0] with DRAM data bus MD[31:0]. This application can be used in desktop systems when CPU data bus loading is concerned. It can also be used in portable system design to isolate 3V CPU data bus GD[31:0] with 5V DRAM data bus MD[31:0].

4. 5V/3V CPU interface select:

(a) MWEJ (pin 67) of M1489 : pull high
CMPGNTJ (pin 43) of M1487 : pull high

When 5V CPU interface is selected, CPU command, address, data, and cache interface (pins 1-48, pins 157-207 of M1489, pins 16-39 of M1487) are defined as 5V.

(b) MWEJ (pin 67) of M1489: pull low
CMPGNTJ (pin 43) of M1487: pull low

When 3V CPU interface is selected. CPU command, address, data, and cache interface (pins 1-48, pins 157-207 of M1489, pins 16-39 of M1487) are defined as 3V. Vcc (pin 22, pin 182 of M1489, pin 40 of M1487) should be connected to 3V power.

5. RESET signals connection:

(a) L1WB or SMI CPU
In a L1WB or SMI-supported CPU systems, the CPU INIT(or SRESET) pin should be connected to the M1487 CPURST pin (pin 20), and the CPU RESET pin connected to the M1487 SYSRST pin (pin 63) shared with the ISA slot RSTDRV signal. And, the M1487 SYSRSTJ pin (pin 81) has the same timing and specification but with an inversed polarity with the SYSRST pin of M1487. The M1489 RSTDRV pin (pin 131) should be connected to the M1487 SYSRST pin.

(b) L1WT or non-SMI CPU
In a L1WT or non-SMI-supported CPU systems, the CPU RESET pin should be connected to the M1487 CPURST pin (pin 20). The M1487 SYSRST pin (pin 63) should be connected to the ISA slot RSTDRV signal and the M1489 RSTDRV pin (pin 131). And, the M1487 SYSRSTJ pin (pin 81) has the same timing and specification but with an inversed polarity with the SYSRST pin of M1487.

6. SMI signals connection:

(a) Intel™ SL-enhanced compatible CPUs:
The SMIACTJ pin of CPU should be connected to the M1489 pin 192. The SMIJ pin of CPU should be connected to M1487 pin 19. The STPCLKJ pin of CPU should be connected to M1487 pin 21.

(b) AMD/Cyrix/TI compatible CPU:
The SMIADSJ pin of CPU should be connected to the M1489 pin 192. The SMIJ pin of CPU should be connected to M1487 pin 19. The SUSPENDJ pin of CPU(Cyrix/TI) should be connected to M1487 pin 21.

7. Power Control Logic:

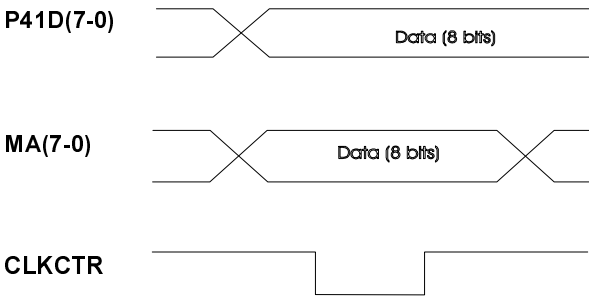
(1) Latched Power Control:
The M1489/M1487 provides 8 programmable output control latched signals (from the XMA[7-0] _ pins 49-51, 54-58 of M1489) for peripheral devices to control power sourcing, or for the external clock synthesis to change its frequency setting. During the power-on reset period, the XMA pins of M1489 will become input polarity to strobe the initial value of power control and the CLKCTR pin of M1487 will become low logic to make the power default setting be transparent for latched element. These values can be read from the register index-41H. This writeable register also can be outputted to the power control signals via a proper programming procedure.

(a) bits mapping:

XMA7 -6 -5 -4 -3 -2 -1 -0

P41D7 -6 -5 -4 -3 -2 -1 -0
(PxxDy : Index - xxH , bit y)

(b) Timing Diagram:



(2) Level Power Control:
The M1489/M1487 also provides 1 simplified programmable output control level-indicating signal, CLKCTR, for peripheral device to control power sourcing, or for the external clock synthesis to change its frequency setting. This control indicating value can be read from the register index-40H D1. This Index-40h D0 data programming can be outputted to control the power-control device via the CLKCTR signal.

8. X-device(ROM/RTC/KBC) control logic of M1487:

(1) Crystal 32.768KHz of internal RTC connection:
The OSC1 (pin 14) and OSC2 (pin 15) of M1487 are the crystal inputs and provided for an external 32.768KHz quartz crystal. In the absence of a crystal, an oscillator output output of 32.768KHz may be fed into OSC1 input.

(2) External RTC Chip select signal connection:
The ENRTC/RTCSJ (pin 71) is used to indicate the internal RTC enable or disable. When this pin is pulled-up during the cold reset period, the internal RTC will be enabled. When this pin is pulled-down during the cold reset period, the internal RTC will be disabled and this pin (pin 71 of M1487) function will be changed to RTC chip select (RTCCSJ) signal.

(3) External KBC Chip select signal connection:
The XBUSCSJ (pin 73) is used to control the KBC Chip select signal for the external keyboard controller when the internal KBC is disabled. The XBUSCSJ is also used to control the ROM Chip select (ROMCSJ) signal.

(4) IRQ1/KBINH control signal connection:

(a) M1487 internal KBC is disabled :
The pin 11 of M1487 should be connected to the IRQ(P24/OB) pin of external KBC and work as the KBC interrupt function when the internal KBC is disabled.

(b) M1487 internal KBC is enabled:
But, the pin 11 of M1487 should be connected to the KBD_INH pin of the keyboard connector and work as the keyboard inhibition function when the internal KBC is enabled.

Section 3: Functional Description

The M1489 and M1487 chip set is designed for all 486-class CPUS including Intel 486SX/487SX, 486DX, 486DX2, P24C/T/D, AMD X5 and 486 CPUs, and Cyrix CX486S (M6/M7). It supports PCi systems with speeds of up to 133MHz. Under green feature, the FINALi-486 chip set can perform Intel S-series or Cyrix or AMD CPUs which support SMM feature. This new generation core logic chip set solution offers the most cost-effective system integration for 486-class systems.

The M1489 (Cache, Memory, PCI controller) chip behaves as a high performance memory and PCI control system. With the integration of Cache/Memory controller, CPU to PCI posted write/read buffer, high speed local bus IDE controller, and sophisticated PCI control interface, it achieves the goal of being the most cost-effective and high-efficiency memory/PCI approach.

The M1487 (ISA Bridge Controller) chip provides the standard ISA control lo9gic and offers an efficient power management unit. For highly cost-effective integrated systems, the M1487 has built-in to the M1487 the RTC, KBC and most ISA buffers.

The chip set incorporates the following functional blocks:

M1489

- CPU interface logic
- Memory logic
- Cache logic
- Memory address decode logic
- Configuration register
- SMM logic control
- Parity checking and parity-generation logic
- CPU to PCI command translation
- PCI to CPU command translation
- CPU to PCI posted write buffer
- CI interface logic
- PCI configuration slave
- PCI to Local Memory write-buffer
- PCI to Local Memory read-buffer
- IDE interface
- Linkbus interface logic

M1487

- Reset control logic and system clock generator
- Linkbus interface logic
- Numeric coprocessor and CPU interface logic
- ISA bus control logic
- PCI master arbiter logic
- PIC IRQ routing logic
- Control logic
- Configure register
- Address buffer
- Data buffer
- Keyboard, RTC and speaker control logic
- ISSP (two 82C37, two 82C59, one 82C54)
- Internal RTC and logic
- Internal KBC and logic
- STPCLKJ control and clock throttling logic
- SMI control logic
- APM control logic
- PMU control logic

The following section describes the blocks of the M1489.

CPU Interface Logic
The CPU interface logic communicates the processor handshaking signals with 486/X5 CPUs. It will handle all of the CPU-side instruct events and requests the bus ownership from the CPU.

Memory Logic
The memory Logic is capable of accessing up to 128MB of local memory, and supporting 4-banks of DRAM using 256K, 512K, 1M, 4M, and 16M single-sided SIMMs. Each bank also supports advanced EDO DRAM individually. Programmable DRAM timing is provided for RAS precharge time and RAS-to-0CAS delay to achieve highest performance and reliability. Programmable shadowing regions are divided into non-cacheable and optional non-cacheable groups. And the CPUs which support write-back will force the shadowing region to non-cacheable mode.

Cache Logic
The cache control uses direct-map, write-back-update methods for maximum performance. Designers can use 32Kx8, 64Kx8 and 128Kx8 SRAMs to form 128K to 1M cache memory size with one-bank or two-bank types. When two-baqnk type is selected, bank interleave is used to increase system performance. 7-bit or 8-bit TAG can also be selected and the dirty bit SRAM is not needed.

Memory Address Decode Logic
The decode-circuit decodes the local memory, shadow RAM and SMRAM region.

Configuration Register
The configuration register controls the whole system at different CPUs under different frequencies. It enables the system to set these configuration registers to meet the compatible, reliable performance and functional requirements.

SMM Logic Control
SMM Logic handles the memory mapping function when SMI even active. And it is different for Intel, Cyrix, and AMD CPU systems. The SMRAM size can be reserved for 128K. The SMRAM address can be redirected to A/B/E region memory location. The SMRAM can be programmed to access directly without SMI event active.

Parity Checking and Parity-Generation Logic
During a local memory-read cycle, the M1489 not only monitors bus steering, but also checks the parity bit for each data byte from DRAM to ensure the correct data is read. If a parity error occurs, the M1487 generates an NMI-interrupt to CPU for the parity error. The parity-check can be disabled by programming index 1Bh. During a local memory write cycle, M1489 monitors the bus steering and uses the accepted data to generate the parity bits sent to DRAM for each data byte.

CPU to PCI Command Translation
This block translates the CPU-bus command to PCI command. It also provides 2 mechanisms for the CPU to generate PCI configuration cycles. The CPU special cycle and INTACK cycle will not broadcast to PCI bus.

PCI to CPU Command Translation
This block translates the PCI command to the CPU command to CPU-bus. But the PCI special cycle, INTACK cycle and configuration cycle will not broadcast to CPU bus.

CPU to PCI Posted Write-Buffer
This block contains four deep write-buffers to improve the CPU to PCI performance. With these write-buffers, the PCI burst-write cycle and fast-back-to-back cycle is made possible. The architecture of the Write-Buiffer is “4 address buffers plus 4 data buffers,” so it can buffer up to 4 consecutive 32-bit write cycles.

PCI Interface Logic
The PCI interface logic communicates the PCI handshaking signals with PCI system. It will broadcast CPU-bus cycle to PCI cyel and repsonse proper activity to PCI master cycle.

PCI Configuration Slave
All PCI configuration registers of the M1489 are contained in this block. It acts as a simple PCI slave.

PCI to Local Memory Posted Write-Buffer
This block contains two line write-gbuffers ot improve the PCI-to-Local memory performance. With these write-buffers, the PCI Master write burst cycle to local memory is made possible. The architecture of the Write-Buffer is “2 address buffers plus 8 data buffers,” so it can buffer up to 8 consecutive 32-bit write cycles.

PCI to Local Memory Read-Buffer
This block contains read-prefetch-buffer to improve the PCI-to-Local memory performance.

IDE Interface
This block provides the highly efficient IDE interface. It can attach four IDE devices and provides fast access for each device. Each device access timing can be programmed differently through separate registers. The built-in enhanced IDE controller provides 4-layer 32-bit posted write-buffer and 4-layer 32-bit read-prefetch-buffer to win the IDE boost performance improvements.

Linkbus Interface Logic
The linkbus interface logic is to control the handshaking signals with the M1487. This block issues the linkbus signals in CPU/PCI master period to M1487 for ISA access cycles. It also receives the linkbus signals from the M1487 in DMA/ISA master period for local memory access cycles.

The following section describes the blocks of the M1487.

Reset Control Logic and System Clock Generator
There are two clock inputs in the M1487. There are CPUCLK/PCICLK clocks which provide frequency operation for the system board, CPU and PCI system. The other is OSC crystal or oscillator which is used as a clock for reset and time-out counters. The ATCLK clock (ATCLK) output is generated from CPUCKL (divided by 4, 5, 6 8) or from OSC (divided by 2). It can be programmed in index 29h. The keyboard controller clock is the same as ATCLK. The switching power supply sends a POWERGOOD signal to the M1487 to generate system-reset and reset the chipsets to initial state.

Linkbus Interface Logic
The linkbus interface logic is used to control the handshaking signals with the M1489. This block receives the M1487 linkbus signals in CPU/PCI master period for ISA access cycles. It also issues the linkbus signals to the M1487 in DMA/ISA master period for local memory access cycles.

Numerical Coprocessor & CPU Interface Logic
When FERRJ signal of CPU is active, this indicates that an unmaskable coprocess exception has occurred and M1487 will generate an IRQ13 to the CPU. Furthermore, the M1487 will drive IGNNEJ active to CPU after a port F0h write access. The M1487 also controls A20MJ/INTR/NMI interface logic and timing to the CPU.

ISA Bus Control Logic
This block includes the ISA bus state machine, 16-bit or 8-bit commands justified wait-state and control logic. These signals are compatible with PC/AT standards.

PCI Master Arbiter Logic
This block arbitrates the requests and grants up to three PCI masters. It supports two rotate priority mode for maximum compatibility and performance.

PCI IRQ Routing Logic
This block provides the remapping (rounding) function from 4 PCI interrupt request lines to 11 ISA interrupt request lines. It can convert the PCI level-sensitive interrupt line to PC/AT edge-sensitive interrupt line.

Control Logic
The control logic controls the internal data bus and address bus flow. It also generates proper read-select to internal device and chooses the correct data output. It selects the correct address bus for DMA and REFRESH cycles to send to the system.

Configure Register
The configure register controls the whole system at different CPUs under different frequencies. It enables the system to set these configuration registers to meet the compatible, reliable performance and functional requirements.

Address Buffer
The address buffer generated at address LA23-LA17, SA19-SA0 and BHEJ for ISA bus, initiates the byte-enable signal at DMA and MASTER cycles.

Data Buffer
The data control signal controls data-transfer between the Linkbus data and ISA data bus during CPU/PCI cycles, DMA cycles and MASTER cycles.

Keyboard, RTC and Speaker Control Logic
This block emulates the keyboard controller, fast-RC and fast gate-A20 functions for maximum performance. It will generate the RTCAS, RTCDS, and RTCWRJ for RTC use. It combines with port61H at this block to generate speaker signal.

ISP Devices (82C37x2, 82C59x2, 82C54, 74LS612)
The ISP device is built-in, thus no 82C206 is required. There are two 82C37's, two 82C59's, one 82C54 and one 74LS612 devices built-in. The 82C59's will support the level-sensitive active low interrupt request feature via properly programming the port 4D0h and 4D1h for slave interrupt controller. These registers are used to set the interrupts to be triggered by either the signal edge or the logic level. IRQ0, IRQ1, IRQ2, IRQ8J, IRQ13 must be set to edge sensitive for AT traditional usage. After the system reset, all IRQ signals are set to edge sensitive. The description below shows which bit numbers represent the various IRQ signals. (0=edge sensitive; 1=level sensitive.)

Port 04D0h	(R/W) 00h
D0	IRQ0
D1	IRQ1
D2	IRQ2
D3	IRQ3
D4	IRQ4
D5	IRQ5
D6	IRQ6
D7	IRQ7

PORT 04d1H	(R/W) 00h
D0	IRQ8J
D1	IRQ9
D2	IRQ10
D3	IRQ11
D4	IRQ12
D5	IRQ13
D6	IRQ14
D7	IRQ15

Internal RTC
The RTC device is built-in, thus no external RTC is required. If the designer chooses not to use the RTC, it can be disabled by hardware setting.

Internal KBC
The KBC (keyboard controller) device is built-in thus no external KBC is required. It can be disabled by hardware setting if not used. The integrated KBC is a AT keyboard controller. If PS/2 is required an external KBC should be used.

Stop Clock Control and Clock Throttling Logic
The STPCLKJ_ signal can be asserted by software setting and will be de-asserted by optional IRQ, IRQ, NMI and SMI events. The M1487 also provides the clock throttling feature so when the INTR, DRQ, NMI or SMI have been idle for a defined period of time, the STPCLKJ_ like signal will be asserted until a new INTR, IRQ, NMI or SMI event occurs. The asserted STPCLKJ_ like signal will not break the pre-asserted INTR, NMI, SMI but it will pend the later INTR, NMI and SMI until STPCLKJ_ like signal is de-asserted.

SMI Control Logic
The SMI request is generated by the programmable events and will record its related cause-code in the local configuration port. The SMI request can be issued to the processor via SMIJ, NMI, IRQ15 or IRQ10 signal. This block will control the SMI I/O drive timing to fit all of the processors including Intel, AMD, and Cyrix's CPU. The SMI request will interlock with the CPU reset signal. The SMI request also drives the A20MJ to inactive state before the entry to SMM and returns to its original level after the last cycle of the SMM state restore. The M1487's SMIJ will be asserted periods prior to asserting the CPURDYJ signal in order to guarantee the processor's recognition on an I/O trap instruction boundary.

APM Control Logic
The APM (Advanced Power Management Interface) creates an interface to allow the Operating System to communicate with the SMM code. The M1487 provides the Index Local Port 30h D5 to generate the software STPCLKJ signal and the Index Local Port 30h D3 to generate the software SMIJ signal for the APM applications.

PMU Control Logic
The PMU (Power Management Unit) can control and dramatically reduce overall system power consumption. This reduction is accomplished via the activity monitors which detect the system inactivity timer timeout and to slow down the clock frequency or to remove the power sources from various peripherals. The M1487 provides three timers from one second to 320 minutes to individually monitor the system state (ON/DOZE/STANDBY/SUSPEND modes), one programmable region, and the standard input devices (such as mouse, keyboard, etc.) activity.

The M1487 can optionally monitor the keyboard, VGA, HDD, FDD, LPT, COM, IRQs, DRQs, PCI masters and two programmable regions of each system state. The M1487 can provide an LED flash control to indicate the system state status. The M1487 also provides 8 programmable output control signals via M1489 MA signals for peripheral devices to control their power sourcing or for the external clock synthesis to change its frequency setting. The M1487 also supports the external switch (suspend button), RTC alarm wakeup control.

Section 4: Configuration Registers

M1489/M1487 Configuration Registers Description

I. Unlock registers sequence:

Step 1: Write I/O port 22h, data 03h
Step 2: Write I/O port 23h, data C5h

Program registers sequence:

Step : Write I/O port 22h, data xxh
(xxh=register index for selecting the register index)

Step 2: Write I/O port 23h, data yyh for register modification
(yyh = modified configuration data)
or, Read I/O port 23h, (data input zzh) for register status read

II. Registers Description:

Note:

(1) All reserved registers and reserved bits should be kept on their own default value for system to operate properly.
(2) The value (**) shown on the bit number column is the bit's default value.

(a) Hardware setting & Lock register:

Register Name: IBC(M1487) Hardware Register
Register Index: 01h
Default Value: 0Fh
Attribut: Read Only

Bit No.	Bit Function
0 (1)	0 : 16 bit ROM select 1 : 8 bit ROM select
1 (1)	0 : Disable built-in RTC function 1 : Enable built-in RTC function
2 (1)	0 : Disable built-in KBC function 1 : Enable built-in KBC function
3 (1)	0 : PCICLK is half of CPU clock 1 : PCICLK is same as CPU clock
4 - 6	D6~D4="000" : IBC(M1487) A0 version ID
7 (0)	0 : 5V Processor interface select 1 : 3.3V Processor interface select

Detailed Bit Description:

Bit No.	Description
0	M1487 will sense XBUSCSJ(pin 73) logic value during the power-on reset period. When it be pulled-up, the system will be recognized as a 8-bit ROM system and this bit will return a 1 when read. When it be pulled-down, the system will be recognized as a 16-bit ROM system and this bit will return a 0 when read.
1	M1487 will sense ENRTC(pin 71) logic value during the power-on reset period. When it be pulled-up, the chip built-in RTC function will be enabled and this bit will return a 1 when read. When it be pulled-down, the chip built-in RTC function will be disabled and this bit will return a 0 when read.
2	M1487 will sense IBCSTJ(pin 42) logic value during the power-on reset period. When it be pulled-up, the chip built-in KBC function will be enabled and this bit will return a 1 when read. When it be pulled-down, the chip built-in KBC function will be disabled and this bit will return a 0 when read.
3	M1487 will sense CMPSTJ(pin 45) logic value during the power-on reset period. When it be pulled-up, the PCI system frequency will be recognized as the same frequency of the CPU processor bus and this bit will return a 1 when read. When it be pulled-down, the PCI system frequency will be recognized as the half frequency of the CPU processor bus and this bit will return a 0 when read.
4 - 6	M1487 Chip version ID.
7	M1487 will sense CMPGNTJ(pin 43) logic value during the power-on reset period. When it be pulled-up, the CPU interface is a 5V or 5V-tolerance processor and this bit will return a 0 when read. When it be pulled-down, the CPU interface is a pure 3.3V processor and this bit will return a 1 when read.

Register Name: CMP(M1489) Hardware Register
Register Index: 02h
Default Value: 0Fh
Attribute: Read Only

Bit No.	Bit Function
0 (1)	0 : PCICLK is half of CPU clock 1 : PCICLK is same as CPU clock
1 (1)	0 : Memory parity data pin supported 1 : External cache chip select pin supported
2 (1)	0 : Memory data buffer control supported 1 : PCI parity error detect pin supported
3 (1)	0 : 3.3V Processor interface select 1 : 5V Processor interface select
4 - 7	D7~D4="0000" : CMP(M1489) A0 version ID

Detailed Bit Description:

Bit No.	Description
0	M1489 will sense CMPSTJ(pin 152) logic value during the power-on reset period. When it be pulled-up, the PCI system frequency will be recognized as the same frequency of the CPU processor bus and this bit will return a 1 when read. When it be pulled-down, the PCI system frequency will be recognized as the half frequency of the CPU processor bus and this bit will return a 0 when read.
1	M1489 will sense CLEAROKJ(pin 153)logic value during the power-on reset period. When it be pulled-up, the M1489 Pin 193/195/198/202 will work functionally as external cache chip select(CCSJ) and this bit will return a 1 when read. When it be pulled-down, these M1489 pins will work as the DRAM parity data pins function and this bit will return a 0 when read.
2	M1489 will sense PCIPERRJ(pin 138)logic value during the power-on reset period. When it be pulled-up, the M1489 pin 138 will work as the PCI parity check pin function and this bit will return a 1 when read. When it is pulled-down, the M1489 pin 138 will work as the 3-5V CPU(Host)_3V and DRAM_5V data buffer control function and this bit will return a 0 when read.
3	M1487 will sense MWEJ(pin 67) logic value during the power-on reset period. When it be pulled-up, the CPU interface is a 5V or 5V-tolerance processor and this bit will return a 1 when read. When it be pulled-down, the CPU interface is a pure 3.3V processor and this bit will return a 1 when read.
4 - 7	M1489 Chip version ID.

Register Name: Lock Register
Register Index: 03h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 7 (00h)	D7~D0="C5h" : M1487 and M1489 system configuration registers are unlocked else : M1487 and M1489 system configuration registers are locked

Detailed Bit Description:

Bit No.	Description
0 - 7	When this register is written as the unlocked logic value -C5h, the M1487 and M1489 system configuration registers can be accessible via a proper Index(22h)/Data(23h) programming sequence. But, if this register is written as the other logic value(except C5h), the M1487 and M1489 system configuration registers will be locked and become inaccessible even using the Index(22h)/Data(23h) programming sequence.

(b) DRAM & Cache Controllers feature:

Register Name: DRAM Configuration Register I
Register Index: 10h
Default Value: F1h
Attribute: Read/Write

Bit No.	Bit Function		
0 - 3 (1h)	DRAM configuration of Bank 0		
	D3 -2 -1 -0	DRAM	Config.(RMA/CMA)
	1 1 1 1	None	None
	0 0 0 0	1M	256Kx1 (9 / 9)
	0 0 0 1	4M	1Mx1 (10/ 10)
	0 0 1 0	2M	512Kx8 (9 / 10)
	0 0 1 1	16M	4Mx1 (11/ 11)
	0 1 0 0	64M	16Mx1 (12/ 12)
	0 1 0 1	8M	2Mx8 (11/ 10)
	0 1 1 0	16M	4Mx4 (12/ 10)
	0 1 1 1	8M	2Mx8 (12/ 9)
	1 0 0 0	4M	1Mx16 (12/ 8)
	(else)	reserved	reserved
4 - 7 (Fh)	DRAM configuration of Bank 1 (bits' definition is the same as D0~D3)		

Note: RMA is the row address number of memory device,
CMA is the column address number of memory device.

Detailed Bit Description:

Bit No.	Description
0 - 3	These 4 bits define the DRAM configuration of bank 0. The memory address mapping definition is described in the MA table. Please refer to the Design Issue section.
4 - 7	These 4 bits define the DRAM configuration of bank 1. The memory address mapping definition is described in the MA table. Please refer to the Design Issue section.

Register Name: DRAM Configuration Register II
Register Index: 11h
Default Value: FFh
Attribute: Read/Write

Bit No.	Bit Function
0 - 3 (Fh)	DRAM configuration of Bank 2 D3 -2 -1 -0 DRAM Config.(RMA/CMA) 1 1 1 1 None None 0 0 0 0 1M 256Kx1 (9/9) 0 0 0 1 4M 1Mx1 (10/10) 0 0 1 0 2M 512Kx8 (9/10) 0 0 1 1 16M 4Mx1 (11/11) 0 1 0 0 64M 16Mx1 (12/12) 0 1 0 1 8M 2Mx8 (11/10) 0 1 1 0 16M 4Mx4 (12/10) 0 1 1 1 8M 2Mx8 (12/9) 1 0 0 0 4M 1Mx16 (12/8) (else) reserved reserved
4 - 7 (Fh)	DRAM configuration of Bank 3 (bits' definition is same as D0~D3)

Note: RMA is the row address number of memory device,
CMA is the col. address number of memory device.

Detailed Bit Description:

Bit No.	Description
0 - 3	These 4 bits define the DRAM configuration of bank 2. The memory address mapping definition is described in the MA table. Please refer to the Design Issues section.
4 - 7	These 4 bits define the DRAM configuration of bank 3. The memory address mapping definition be described in the MA table. Please refer to the Design Issues section.

Register Name: ROM Function Register
Register Index: 12h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	E(0E0000h~0EFFFFh) region cycle definition 0 : E region not be on-board ROM region 1 : E region be on-board ROM region
1 (0)	CL(0C0000h~0C7FFFh) region cycle definition 0 : CL region not be on-board ROM region 1 : CL region be on-board ROM region
2 (0)	CH(0C8000h~0CFFFFh) region cycle definition 0 : CH region not be on-board ROM region 1 : CH region be on-board ROM region
3 (0)	15M(0F00000h~0FFFFFFh) region definition 0 : 15M region not be specified to ISA usage 1 : 15M region be specified to ISA range
4 (0)	Flash ROM writing supported feature 0 : disable flash ROM supported feature 1 : enable flash ROM supported feature
5 (0)	CMP swap MIOJ definition in special cycle 0 : disable swap MIOJ in special cycle 1 : enable swap MIOJ in special cycle (related to Index-45h D5)
6 (0)	DRAM RAS signal active timeout check feature 0 : disable RAS timeout check feature 1 : enable RAS timeout check feature
7 (0)	DRAM hidden refresh feature 0 : disable DRAM hidden refresh feature 1 : enable DRAM hidden refresh feature

Note: Please refer to Index-44h D7~D6 for D-region on-board ROM use.

Detailed Bit Description:

Bit No.	Description
0	This bit is used to recognize the on-board ROM with E (0E0000h~0EFFFFh) region feature. When it be set to 1, the E region memory cycle will be treated as the on-board ROM access cycle. And, the ROMCSJ will be asserted in the E-region memory assess cycle. Otherwise, the E- region memory cycle will be treated as a normal ISA access cycle.
1	This bit is used to recognize the on-board ROM with C- lower(0C0000h~0C7FFFh) region feature. When it be set to 1, the C-lower memory region cycle will be treated as the on-board ROM access cycle. And, the ROMCSJ will be asserted in the C-lower region memory assess cycle. Otherwise, the C-lower region memory cycle will be treated as a normal ISA access cycle.
2	This bit is used to recognize the on-board ROM with C- upper(0C8000h~0CFFFFh) region feature. When it be set to 1, the C-upper memory region cycle will be treated as the on-board ROM access cycle. And, the ROMCSJ will be asserted in the C-upper region memory assess cycle. Otherwise, the C-upper region memory cycle will be treated as a normal ISA access cycle.
3	This bit is used to locate the 15M (0F00000h~ 0FFFFFFh) memory region. When it be set to 1, the 15M memory access cycle will always be treated as the ISA range (even under on-board DRAM exceeded 15M condition). Otherwise, the 15M memory use will be treated as the normal access cycle.
4	This bit is used to support the flash ROM feature. When it is set to 1, the ROM chip select signal will be asserted in the ROM region write access cycle. Otherwise, the ROM chip select signal will not be asserted in the ROM region write access cycle.
5	This bit is used to swap the MIOJ signal in the CPU special cycle decoding. When it be set to 1, the CPU special cycle will be recognized as the Memory-Code-Write access cycle. Otherwise, the CPU special cycle will be recognized as the I/O-Code-Write access cycle. This bit should be programmed in the same definition as the Index- 45h D5 for system consistency.
6	This bit is used to control the DRAM RAS signal active timer timeout feature. When it be set to 1, the DRAM RAS signal active timeout check feature will be enabled. Otherwise, the DRAM RAS signal active timeout check feature will be disabled.
7	This bit is used to control the DRAM hidden refresh feature. When it is set to 1, the DRAM hidden refresh feature will be enabled. Otherwise, the DRAM hidden refresh feature will be disabled.

Register Name: Shadow Region Register
Register Index: 13h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	0C0000h~0C3FFFh region shadow control 0 : disable 0C0000h~0C3FFFh in shadow region 1 : enable 0C0000h~0C3FFFh in shadow region
1 (0)	0C4000h~0C7FFFh region shadow control 0 : disable 0C4000h~0C7FFFh in shadow region 1 : enable 0C4000h~0C7FFFh in shadow region
2 (0)	0C8000h~0CBFFFh region shadow control 0 : disable 0C8000h~0CBFFFh in shadow region 1 : enable 0C8000h~0CBFFFh in shadow region
3 (0)	0CC000h~0CFFFFh region shadow control 0 : disable 0CC000h~0CFFFFh in shadow region 1 : enable 0CC000h~0CFFFFh in shadow region
4 (0)	0D0000h~0D3FFFh region shadow control 0 : disable 0D0000h~0D3FFFh in shadow region 1 : enable 0D0000h~0D3FFFh in shadow region
5 (0)	0D4000h~0D7FFFh region shadow control 0 : disable 0D4000h~0D7FFFh in shadow region 1 : enable 0D4000h~0D7FFFh in shadow region
6 (0)	0D8000h~0DBFFFh region shadow control 0 : disable 0D8000h~0DBFFFh in shadow region 1 : enable 0D8000h~0DBFFFh in shadow region
7 (0)	0DC000h~0DFFFFh region shadow control 0 : disable 0DC000h~0DFFFFh in shadow region 1 : enable 0DC000h~0DFFFFh in shadow region

Detailed Bit Description:

Bit No.	Description
0	The 0C0000h~0C3FFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
1	The 0C4000h~0C7FFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
2	The 0C8000h~0CBFFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
3	The 0CC000h~0CFFFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
4	The 0D0000h~0D3FFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
5	The 0D4000h~0D7FFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
6	The 0D8000h~0DBFFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
7	The 0DC000h~0DFFFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.

Register Name: Shadow Control Register
Register Index: 14h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	0E0000h~0E7FFFh region shadow control 0 : disable 0E0000h~0E7FFFh in shadow region 1 : enable 0E0000h~0E7FFFh in shadow region
1 | (0)	0E8000h~0EFFFFh region shadow control 0 : disable 0E8000h~0EFFFFh in shadow region 1 : enable 0E8000h~0EFFFFh in shadow region
2 (0)	0F0000h~0F7FFFh region shadow control 0 : disable 0F0000h~0F7FFFh in shadow region 1 : enable 0F0000h~0F7FFFh in shadow region
3 (0)	0F8000h~0FFFFFh region shadow control 0 : disable 0F8000h~0FFFFFh in shadow region 1 : enable 0F8000h~0FFFFFh in shadow region
4 (0)	Shadow region read control feature 0 : disable shadow region read feature 1 : enable shadow region read feature
5 (0)	Shadow region write control feature 0 : disable shadow region write feature 1 : enable shadow region write feature
6 - (0)	reserved
7 (0)	Write 1 to improve DX4-100 2-1-1-1 reliability

Detailed Bit Description:

Bit No.	Description
0	The 0E0000h~0E7FFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
1	The 0E8000h~0EFFFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
2	The 0F0000h~0F7FFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
3	The 0F8000h~0FFFFFh ISA memory region will be treated as local shadow RAM region when this bit is set to 1.
4	The shadow ISA memory region read access cycle will be treated as local shadow RAM cycle when this bit is set to 1.
5	The shadow ISA memory region write access cycle will be treated as local shadow RAM cycle when this bit is set to 1.
6	This bit should be kept logic 0 for system work properly.
7	Fix this bit to 1.

Register Name: Cycle Check Point Control Register
Register Index: 15h
Default Value: 20h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	Cyrix linear address supported 0 : disable Cyrix linear address support 1 : enable Cyrix linear address support
1 - 3	reserved
4 - 5 (D5D4) (10)	CPU Cycle check point select D5D4: check point 00 : T1 end 01 : T2 end 10 : T3 end 11 : reserved
6 - 7 (0h)	Master Cycle check point select D7D6: check point 00 : T1 end 01 : T2 end 10 : T3 end 11 : reserved

Detailed Bit Description:

Bit No.	**Description**
0	This bit is used to support the Cyrix linear burst address feature for improving the CPU internal cache performance.
1 - 3	These bits must be kept to 0 for system normal operation.
4 - 5	These bits are used for M1489 to control the check timing of the DRAM decoding and external cache comparison in the CPU cycles. The slower check point setting implies the more decoding and comparing time for a more stable system. But, the slow check point setting also implies a lower system performance.
6 - 7	These bits are used for M1489 to control the check timing of the DRAM decoding and external cache comparison in the Master cycles. The slower check point setting implies the more decoding and comparing time for a more stable system. But, the slow check point setting also implies a lower system performance.

Register Name: Cache Control Register I
Register Index: 16h
Default Value: 30h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	Internal L1 cache ON/OFF 0 : disable L1 cache 1 : enable L1 cache
1 (0)	External L2 cache ON/OFF 0 : disable L2 cache 1 : enable L2 cache
2 (0)	Internal L1 cache WB/WT feature 0 : L1 write through selected 1 : L1 write back selected
3 (0)	External L2 cache TAG-8bit(force dirty) feature 0 : L2 write back with TAG-7bit selected 1 : L2 write back with TAG-8bit selected
4 (1)	L2 cache controller write timing setting 0 : L2 write fast timing selected 1 : L2 write normal timing selected
5 (1)	L2 cache controller read timing setting 0 : L2 read fast timing selected 1 : L2 read normal timing selected
6 (0)	L2 cache write rising timing setting 0 : normal rising timing setting 1 : early rising timing setting
7 (0)	TAG write rising timing setting 0 : normal rising timing setting 1 : early rising timing setting

Detailed Bit Description:

Bit No.	Description
0 - 3	These 4 bits are used to enable the internal L1 cache and the external L2 cache function. The L1 and L2 cache operating structure is also defined by these bits.
4 - 5	These 2 bits are used to set the L2 cache access timing.
6 - 7	These 2 bits are used to define the L2 cache and TAG SRAM write rising timing scheme for an adequate cache or TAG data hold time.

Register Name: Cache Control Register II
Register Index: 17h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 1 (0h)	L2 cache SRAM type configuration D1D0:SRAM configuration 00 : reserved 01 : 32K * 8 SRAM 10 : 64K * 8 SRAM 11 : 128K * 8 SRAM
2 (0)	L2 cache structure 0 : 1 bank L2 cache SRAM 1 : 2 bank L2 cache SRAM
3 (0)	Force L2 cache miss feature 0 : normal operation 1 : force L2 cache MISS
4 (0)	Force L2 cache non-dirty feature 0 : normal operation 1 : force L2 memory cycles be NON-DIRTY
5 (0)	Force L2 cache hit feature 0 : normal operation 1 : force L2 cache HIT
6 (0)	Shadow region L2 cacheable feature 0 : disable shadow region L2 cacheable 1 : enable shadow region L2 cacheable & set to be write-protect
7 (0)	Shadow region data L1 cacheable feature 0 : disable shadow region data L1 cacheable 1 : enable shadow region data L1 cacheable

Detailed Bit Description:

Bit No.	Description
0 - 2	These 3 bits are used to define the L2 SRAM configuration and structure.
3 - 5	These 3 bits are used to size the SRAM range and initialize the L2 SRAM.
6 - 7	These 2 bits are used to control the shadow region L1/L2 cacheable feature.

Register Name: Reserved
Register Index: 18h
Attribute: reserved

Register Name: SMM Control Register
Register Index: 19h
Default Value: 04h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	VGA access in SMM when SMM RAM is set as AB region (index 19H D5D4="01") 0 : disable VGA access in SMM 1 : enable VGA access in SMM
1 (0)	Inserted 1 wait for cycle decoding time 0 : normal cycle checking and decoding timing setting 1 : inserted 1 wait for cycle checking and decoding timing setting
2 (1)	HITMJ sampling timing definition 0 : 2T after EADSJ be asserted 1 : 3T after EADSJ be asserted
3 (0)	Access SMM Memory MAP at normal cycle 0 : Disable SMM memory map at normal cycle Only at SMM mode can access SMM memory 1 : Enable SMM memory map at normal cycle
4 - 5 (0h)	SMM mapping region definition D5D4 : SMM mapping 00 : disable SMM RAM 01 : A,B region 10 : E region 11 : 38000 (68000 for AMD) remapped to AB
6 - 7 (0h)	CPU type selected D7D6 : CPU type 00 : I486(Write-through) supported 01 : Intel Write-back compatible supported 10 : Cyrix supported 11 : reserved

Detailed Bit Description:

Bit No.	Description
0	This bit is used to enable the VGA access in the SMI routine when SMM is mapped in A,B region.
1	This bit is used to increase the cycle checking and decoding time by inserting a wait state for a more stable system.
2	This bit is used to define the HITMJ signal sampling timing of the L1 write-back CPU system.
3	This bit is used to initialize the SMM code of the SMI routine in the normal cycles.
4 - 5	These 2 bits are used to define the SMM mapping region.
6 - 7	These 2 bits are used to define the CPU type.

Register Name: EDO DRAM Configuration Register
Register Index: 1Ah
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	DRAM Bank 0 EDO supported 0 : disable EDO setting in DRAM Bank 0 1 : enable EDO setting in DRAM Bank 0
1 (0)	DRAM Bank 1 EDO supported 0 : disable EDO setting in DRAM Bank 1 1 : enable EDO setting in DRAM Bank 1
2 (0)	DRAM Bank 2 EDO supported 0 : disable EDO setting in DRAM Bank 2 1 : enable EDO setting in DRAM Bank 2
3 (0)	DRAM Bank 3 EDO supported 0 : disable EDO setting in DRAM Bank 3 1 : enable EDO setting in DRAM Bank 3
4 (0)	Enable EDO write 2-1-1-1 timing 0 : disable EDO write timing 1 : enable EDO write timing
5 (0)	Enable EDO test mode 0 : disable EDO test mode 1 : enable EDO test mode
6 - 7 (0)	DRAM hidden refresh period D7D6: refresh period 00 : 15us hidden refresh rate 01 : 30us hidden refresh rate 10 : 60us hidden refresh rate 11 : 120us hidden refresh rate

Detailed Bit Description:

Bit No.	Description
0 - 5	These 6 bits are used to define the EDO configuration and timing. The bit 5 is specially used to size or check EDO DRAM configuration.
6 - 7	These 2 bits are used to set to on-board DRAM hidden refresh rate.

Register Name: DRAM Timing Control Register
Register Index: 1Bh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
1 - 0 (0h)	DRAM read timing selected 00 : slow DRAM read timing setting 01 : normal DRAM read timing setting 10 : fast DRAM read timing setting 11 : fastest DRAM read timing setting
3 - 2 (0h)	DRAM write timing selected 00 : slow DRAM read timing setting 01 : normal DRAM read timing setting 10 : fast DRAM read timing setting 11 : fastest DRAM read timing setting
4 (0)	RAS-only refresh supported 0 : disable RAS-only refresh supported 1 : enable RAS-only refresh supported
5 (0)	On-board memory parity check feature 0 : disable on-board memory parity check 1 : enable on-board memory parity check
6 - 7 (0h)	CPU time-slot selected for CPU-side ownership controller D7D6: CPU ownership timeslot 00 : 4T 01 : 8T 10 : 16T 11 : 32T

Detailed Bit Description:

Bit No.	**Description**
0 - 3	The DRAM access timing setting is defined on these 4 bits.
4	The DRAM RAS-only or CAS-before-RAS refresh algorithm selection.
5	This bit is used to enable on-board memory parity check feature.
6 - 7	These bits are used to define the bus ownership timeslot of CPU in the system arbitrating scheme to guarantee the CPU performance.

Register Name: Memory Data Buffer Direction Control Register
Register Index: 1Ch
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	Bank0 DRAM position setting 0 : Bank0 DRAM on CPU bus 1 : Bank0 DRAM on MD bus
1 (0)	Bank1 DRAM position setting 0 : Bank0 DRAM on CPU bus 1 : Bank0 DRAM on MD bus
2 (0)	Bank2 DRAM position setting 0 : Bank0 DRAM on CPU bus 1 : Bank0 DRAM on MD bus
3 (0)	Bank3 DRAM position setting 0 : Bank0 DRAM on CPU bus 1 : Bank0 DRAM on MD bus
4 (0)	L2 SRAM position setting 0 : L2 SRAM on CPU bus 1 : L2 SRAM on MD bus
5 - 7 (0h)	reserved

Detailed Bit Description:

Bit No.	Description
0 - 4	These 5 bits are used to define the DRAM/SRAM located bus architecture in the 3/5V mixed bus system. The CPU bus means the 3V system bus. And, the MD bus means the 5V system bus.
5 - 7	These bits must be kept low for normal operation of system.

Register Name: Reserved
Register Index: 1Dh
Attribute: Reserved

Register Name: Linear Wrapped Burst Order Mode Control Register
Register Index: 1Eh
Attribute: Read/Write

Bit No.	Bit Function
0-5(0h)	reserved
6 (0)	Linear wrapped burst order mode support 0 : disable linear wrapped burst mode support 1 : enable linear wrapped burst mode support
7(0)	reserved

Detailed Bit Description:

Bit No.	Description
0-5	These bits must be kept low for normal operation of system.
6	The Cyrix M1SC linear wrapped burst mode (0-4-8-C, 4-8-C-0, 8-C-0-4, C-0-4-8) will be supported when this bit is set to 1.
7	This bit must be kept low for normal operation of system.

Register Name: Reserved
Register Index: 1Fh
Attribute: Reserved

(c) PCI feature:

Register Name: CPU to PCI Buffer Control Register
Register Index: 20h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	Fast dynamic ISA cycle feature 0 : disable the dynamic ISA cycle check 1 : enable the dynamic ISA cycle check
1 (0)	Fast dynamic PCI memory cycle feature 0 : disable dynamic PCI memory cycle check 1 : enable dynamic PCI memory cycle check
2 (0)	CPU to PCI write buffer feature 0 : disable CPU to PCI write buffer 1 : enable CPU to PCI write buffer
3 (0)	CPU to PCI write buffer byte merge feature 0 : disable CPU to PCI write byte merge 1 : enable CPU to PCI write byte merge
4 (0)	CPU to PCI write buffer burst cycle feature 0 : disable CPU to PCI write burst 1 : enable CPU to PCI write burst
5 (0)	CPU to PCI write buffer fast-back-to-back feature 0 : disable write fast-back-to-back 1 : enable write fast-back-to-back
7 - 6 (0h)	PCI VGA memory hole feature D7D6: PCI memory hole 00 : disable 01 : enable memory A0000-AFFFFh PCI hole 10 : enable memory A0000-AFFFFh and B8000- BFFFFh PCI hole 11 : enable memory A0000-AFFFFh and B0000-BFFFFh PCI hole

Detailed Bit Description:

Bit No.	Description
0	This bit used to enable the fast dynamic ISA cycle feature for enhancing the ISA access performance.
1	This bit used to enable the fast dynamic PCI memory cycle feature for enhancing the PCI access performance.
2 - 5	These bits are used to enable the CPU to PCI write buffer feature for improving the CPU to PCI write performance.
6 - 7	These bits are used to define the PCI VGA memory hole feature.

Register Name: DEVSELJ Check Point Setting Register
Register Index: 21h
Default Value: 72h
Attribute: Read/Write

Bit No.	Bit Function
1 - 0 (1h)	DEVSELJ check point selected 00 fast sample point for DEVSELJ 01 typical sample point for DEVSELJ 10 slow sample point for DEVSELJ 11 subtractive sample point for DEVSELJ
2 (0)	Write 1 to improve DX4-100 2-1-1-1 reliability
3 (0)	CPU to PCI read/write cycle address issue 1/2 cycles. 0 : issue 1 cycle for write access 1 : issue 2 cycles for write access
4 (1)	Master abort mode enable/disable selected 0 : enable (the normal 5 clocks termination) 1 : disable (fast termination when no PCI slave response)
5 (1)	A31='1' and A26~A24="111" for ROM recognition 0 : disable A31, A26~A24 for ROM recognition 1 : enable A31, A26~A24 for ROM recognition
6	reserved
7 (0)	Fully I/O decoding for General-Purpose I/O 0 : disable fully I/O decoding for GP/IO 1 : enable fully I/O decoding for GP/IO

Detailed Bit Description:

Bit No.	Description
1 - 0	When M1489 act as a PCI slave, If these two bits are programmed to be "11", the check point will be slow not subtractive.
2	Fix this bit to 1.
3	This bit is used to define the CPU to PCI read/write cycle address issuing timing 1T or 2T.
4	This bit is used to enable the master abort function.
5	This bit is used to define the A31, A26~A24 ROM cycles recognition.
7	The PMU ISA I/O events address decoded range be defined in address line 15 to line 0(SA15 - SA0) when this bit be set to 1. Otherwise, the PMU ISA I/O events address decoded range be defined in address line 9 to line 0.

Register Name: PCI to CPU W/R Buffer Configuration Register
Register Index: 22h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	Disable/Enable PCI to CPU local read buffer 0 : disable PCI to CPU read buffer 1 : Enable PCI to CPU read buffer
1(1)	reserved
2(0)	Write to improve DX4-100 2-1-1-1 reliability.
3(0)	PCI to CPU local memory write buffer burst feature 0 : disable PCI to CPU write burst 1 : enable PCI to CPU write burst
4(0)	Disable/Enable PCI to CPU write buffer 0 : disable PCI to CPU write buffer 1 : enable PCI to CPU write buffer
5(0)	PCI Master write cycle Retry/Wait when PCI to CPU write buffer is full 0 : Wait in PCI to CPU write buffer is full 1 : Retry in PCI to CPU write buffer is full
6(0)	Fast/Normal FRAMEJ generation in non-buffer cycles, when M1489 acts as a PCI Master. 0 : Normal FRAMEJ in non-buffer cycles. 1 : fast FRAMEJ in non-buffer cycles.
7 (0)	Fast/Normal FRAMEJ generation in write buffer cycles, when M1489 acts as a PCI Master and CPU to PCI buffer is enabled. 0 : Normal FRAMEJ in write buffer cycles 1 : Fast FRAMEJ in write buffer cycles

Detailed Bit Description:

Bit No.	Description
0	The bit enables the PCI_MASTER to Host read buffer. And it supports PCI_MASTER to Host read burst also. Then the performance of master will be enhanced.
1	This bit should be kept to 1 for system's normal operation.
2	Fix this bit to 1.
3	This bit supports PCI_MASTER to Host Write buffer can burst write to local memory.
4	The bit enables PCI_MASTER to Host write buffer. And it supports PCI_MASTER to Host write burst also. Then the performance of master will be enhanced.
5	As the PCI_MASTER to Host write buffer is full, the next data transfer will be waiting or retry until buffer be flushed.
6	M1489 supports two FRAMEJ timing as CPU to access PCI. For non_buffer cycle the Fast FRAMEJ select will enhance the performance but the address path delay will influence the system stability.
7	For buffer cycle the FRAMEJ select will influence the next data merge or not. Then the FRAMEJ select will depend on the software operation.

Register Name: Reserved
Register Index: 23h
Attribute: Reserved

Register Name: Reserved
Register Index: 24h
Attribute: Reserved

Register Name: GP/MEM Address Definition Register I
Register Index: 25h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
3 - 0 (0h)	defined memory address mask A31, A26-A24 for PMU GP/MEM 0 : unmask the respective address line 1 : mask respective address line bit 3 : address line A31 bit 2 : address line A26 bit 1 : address line A25 bit 0 : address line A24
7 - 4 (0h)	defined memory address A31, A26-A24 for PMU GP/MEM bit 3 : address line A31 bit 2 : address line A26 bit 1 : address line A25 bit 0 : address line A24

Detailed Bit Description:

Bit No.	Description
7 - 0	These bits are used to define the address range and mask feature of A31, A26-A24 for PMU GP/MEM function.

Register Name: GP/MEM Address Definition Register II
Register Index: 26h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7 - 0 (0h)	defined memory address A23-A16 for PMU GP/MEM bit 7 : address line A23 bit 6 : address line A22 bit 5 : address line A21 bit 4 : address line A20 bit 3 : address line A19 bit 2 : address line A18 bit 1 : address line A17 bit 0 : address line A16

Detailed Bit Description:

Bit No.	Description
7 - 0	These bits are used to define the address range of A23- A16 for PMU GP/MEM function.

Register Name: GP/MEM Address Definition Register III
Register Index: 27h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7 - 0 (0h)	defined memory address mask A23-A16 for PMU GP/MEM 0 : unmask the respective address line 1 : mask respective address line bit 7 : address line A23 bit 6 : address line A22 bit 5 : address line A21 bit 4 : address line A20 bit 3 : address line A19 bit 2 : address line A18 bit 1 : address line A17 bit 0 : address line A16

Detailed Bit Description:

Bit No.	Description
7 - 0	These bits are used to define the address mask of A23- A16 for PMU GP/MEM function.

Register Name: PCI Arbiter Control Register
Register Index: 28h
Default Value: 02h
Attribute: Read/Write

Bit No.	Bit Function
3 - 0 (2h)	PCI Master time slot define for arbiter D3-D0: Time slot 0000 : Timer disable 0001 : 1x32 PCICLKs 0010 : 2x32 PCICLKs 0011 : 3x32 PCICLKs 0100 : 4x32 PCICLKs 0101 : 5x32 PCICLKs 0110 : 6x32 PCICLKs 0111 : 7x32 PCICLKs 1000 : 8x32 PCICLKs 1001 : 9x32 PCICLKs 1010 : 10x32 PCICLKs 1011 : 11x32 PCICLKs 1100 : 12x32 PCICLKs 1101 : 13x32 PCICLKs 1110 : 14x32 PCICLKs 1111 : 15x32 PCICLKs
4 (0)	PCI Master BROKE timer selected 0 : disable PCI Master BROKE function 1 : enable PCI Master BROKE function (IDLE for 16 PCICLKs)
5 (0)	Arbiter mode selected 0 : The rotate is ISA->CPU->PCI0->PCI1->PCI2 ->CPU->ISA->CPU->PCI0.... 1 : The rotate is ISA->CPU->PCI0->CPU->ISA-> CPU->PCI1->CPU->ISA-PCI2->CPU->ISA->CPU->PCI0->....
7 - 6	reserved

Detailed Bit Description:

Bit No.	Description
3 - 0	The time slot is defined how long the PCI_MASTER can assert the system bus.
4	Follow the PCI specification as grant to a PCI_MASTER to assert the PCI_BUS but the PCI_MASTER not access the PCI_BUS after 16 PCICLK then the PCI_MASTER will be broken as abnormal.
5	M1487 supports two arbiter mode for user select. The user can easily select which one is more efficient for different systems.

(d) System feature:

Register Name: System Clock Register
Register Index: 29h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 2 (0h)	AT system clock select setting D2 -1 -0 AT clock frequency 0 0 0 7.16 MHz(OSC_14.318MHz/2) 0 0 1 CPUCLK/3 0 1 0 CPUCLK/4 0 1 1 CPUCLK/5 1 0 0 CPUCLK/6 1 0 1 CPUCLK/8 (else) reserved
3(0)	DMA clock select setting 0 : DMA clock is half of AT system clock 1 : DMA clock is same as AT system clock
4(0)	Port-92h feature control bit 0 : disable Port-92h control feature 1 : enable Port-92h control feature
5 - 6 (0h)	16-bit ISA cycle wait state control D6 D5 16-bit ISA cycle access timing 0 0 Normal ISA access timing 0 1 Insert 1 wait state 1 0 Insert 2 wait states 1 1 Insert 3 wait states
7 (0)	ISA data writing hold time extended feature 0 : disable extended data hold time feature 1 : enable extended data hold time feature

Detailed Bit Description:

Bit No.	Description
0 - 2	These 3 bits are used to select the AT clock setting. The AT clock frequency can be generated by OSC_14.318MHz (divided by 2) or by CPUCLK(divided by a programmed factor).
3	The DMA clock system is generated by the AT clock system. The DMA clock frequency is the same as the AT clock frequency when this bit be set to 1. Otherwise, the DMA clock frequency is the half of the AT clock frequency.
4	This bit is used to control the Port-92h function. The Port-92h feature can be enabled when this bit be set to 1. When the Port-92h feature be enabled, the Gate-A20 and soft-CPU-reset can be controlled via a Port-92h access. The Port-92h function is description as below : Port-92h : Default Value = 24h, Read/Write attribute Bit 0 : Soft-CPU-reset control 0 : allows to trigger a soft-reset 1 : trigger a soft-reset event This bit is set to 0 by the system cold reset. Writing a 1 to this bit will cause a soft reset triggered event. Before another soft reset event can be triggered, this bit should be written back to logic 0. Bit 1 : Gate-A20 control 0 : drives the Gate-A20 to low 1 : drives the Gate-A20 to high Writing logic 0 to this bit will cause the Gate-A20 to be driven low. Writing 1 to this bit will cause the Gate-A20 to be driven high. Bit 7 ~ Bit 2 : These bits are reserved and return logic "001001" when read.
5 - 6	These 2 bits are used to to define the default 16-bit ISA cycle access timing.
7	This bit is used to control the ISA writing data extended feature. The ISA data will be kept at least 1 AT clock after the ISA write command inactive when this bit be set to 1. Otherwise, the ISA data will be kept only at least 1 CPUCLK after the ISA write command inactive.

Register Name: I/O Recovery Register
Register Index: 2Ah
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	I/O recovery feature 0 : disable I/O recovery feature 1 : enable I/O recovery feature
1 - 3 (0h)	I/O recovery time setting D3 D2 D1 I/O recovery time 0 0 0 0 µs 0 0 1 0.5 µs (4*AT_CLK) 0 1 0 1.0 µs (8*AT_CLK) 0 1 1 1.5 µs (12*AT_CLK) 1 0 0 2.0 µs (16*AT_CLK) 1 0 1 2.5 µs (20*AT_CLK) 1 1 0 3.0 µs (24*AT_CLK) 1 1 1 3.5 µs (28*AT_CLK)
4 (0)	Co-processor error interrupt ignored feature 0 : Co-processor error interrupt request will not be ignored 1 : Co-processor error interrupt request will be ignored
5 - 6 (0h)	System refresh period setting D6 D5 System refresh period 0 0 15 µs refresh period 0 1 30 µs refresh period 1 0 60 µs refresh period 1 1 120 µs refresh period
7 (0)	PS/2 mouse present feature 0 : without PS/2 mouse in system 1 : with PS/2 mouse in system

Detailed Bit Description:

Bit No.	Description
0	For some traditional slow respondent I/O devices, an command recovery time between two consecutive I/O access cycle will be inserted when this bit be set to 1. And, the recovery time period is defined in the bit 1 to bit 3.
1 - 3	I/O recovery period time definition
4	The FERRJ active event will cause a coprocessor error interrupt request to the CPU when this bit is set to 0. Otherwise, the FERRJ active event will be ignored by the interrupt controller.
5 - 6	These 2 bits are used to define the system memory refresh period time.
7	When this bit be set to 1, the IRQ12 rising-edge (PS/2 mouse active) event will be latched in the internal interrupt controller until a keyboard controller read access command. Otherwise, the IRQ12 event will be treated as a normal interrupt request event.

Register Name: Turbo Function Register
Register Index: 2Bh
Default Value: DBh
Attribute: Read/Write

Bit No.	Bit Function
0 (1)	Turbo mode HW(hardware button)/SW(software programming) priority setting 0 : HW(turbo button) logic-High higher priority 1 : HW/SW with equal priority
1 (1)	SW turbo function setting control 0 : SW de-turbo setting 1 : SW turbo setting
2 (0)	HW turbo button enable feature 0 : disable HW turbo button response 1 : enable HW turbo button response
3 (Read-Only)	HW turbo button status (It be meaningful only when D2 be set to 1.) 0 : HW turbo button is in de-turbo (Low) 1 : HW turbo button is in turbo (High)
4 (Read-Only)	System turbo performance status 0 : system is in de-turbo (SPLED = OFF) 1 : system is in turbo (SPLED = ON)
5 (0)	Swap address line A16 in E/F ROM region 0 : normal access E/F ROM region 1 : swap address A16 in E/F ROM access
6 (1)	reserved
7 (1)	ISA master cycle read prefetch feature 0 : disable ISA master read prefetch feature 1 : enable ISA master read prefetch feature

Detailed Bit Description:

Bit No.	Description
0	When this bit be set to 0, a Turbo signal pin logic "1" event will force the system operating at a turbo state and inhibit the software turbo/deturbo programming response. But, in the Turbo signal logic "0" state, the software turbo/deturbo programming event will be respondent. When this bit is set to 1, a later turbo/deturbo request whether it be set by hardware Turbo or software programming will overrule the formal system deturbo/turbo state.
1	This bit is used to set the system operation at turbo state when it is set to 1, or set to deturbo state. When it is set to 0. i.e. this is the software turbo/deturbo programming bit.
2	This bit is used to enable the hardware Turbo signal pin input response.
3	This read-only bit is to display the Turbo pin signal status and it is meaningful only when the Turbo response feature be enabled.
4	This read-only bit is to reflect the system operating status. i.e. it is the turbo-LED status report.
5	The system A16 address line signal will be swap its logic from the "1" to "0" or "0" to "1" (from CPU side to ISA slot side) in the E/F ROM access cycles when this bit is set to 1. i.e. the E/F ROM address mapping will swap each other.
6	This bit should be kept on 1 for system normal operation.
7	This bit is used to enable/disable the ISA/DMA master local memory read prefetch feature for improving the ISA/DMA master efficiency.

(e) Green function

Register Name: Power Management Unit Control Register
Register Index: 30h
Default Value : 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 1 (0h)	System state D1 D0 : system state definition 0 0 : ON 0 1 : DOZE 1 0 : STANDBY 1 1 : SUSPEND
2 (0)	PMU feature control 0 : disable the PMU feature 1 : enable the PMU feature
3 (0)	Software SMI 0 : disable software SMI event 1 : asserts software SMI event
4 (0)	SMI event signal 0 : disable or clear the SMI event signal 1 : enable the SMI request event
5 (0)	STPCLKJ control 0 : disable STPCLKJ event 1 : asserts software STPCLKJ event
6 (0)	DMA/ISA/PCI Master request de-assert STPCLKJ 0 : Master request will de-assert STPCLKJ 1 : Master request will not de-assert STPCLKJ
7 (0)	IRQ/NMI request de-assert STPCLKJ 0 : IRQ/NMI request will de-assert STPCLKJ 1 : IRQ/NMI request will not de-assert STPCLKJ

Detailed Bit Description:

Bit No.	Description
0 - 1	These 2 bits are used to identify the system power control state by the software programmer. There are no specific hardware implementation in the real circuit design.
2	This bit is used to control the system power management unit function be enabled or disabled.
3	Writing a 1 to this bit will cause a software SMI event to be issued when the PMU and SMI event be enabled. Before another SMI(including the software SMI) event can be issued, this bit must be written back to a 0.
4	This bit is used to control the SMI event function. The SMI signal or events can be issued only when this bit be set to a 1. Otherwise, writing a 0 to this bit will cause the present SMI event to be cleared and the next SMI events to be blocked or disabled.
5	Writing a 1 to this bit will cause a Stop-Clock active event to be issued when the PMU function is enabled.
6	The DMA, ISA masters, or PCI masters request events will break the Stop-Clock active status when this bit is set to 0. Otherwise, a Stop-Clock active event will not be broken by the DMA, ISA masters, or PCI masters request events.
7	The IRQ or NMI request events will break the Stop-Clock active status when this bit is set to 0. Otherwise, a Stop-Clock active event will not be broken by the IRQ or NMI request events.

Register Name: Mode Timer Monitoring Events Selection Register I
Register Index: 31h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	KBD selected (60h, 64h) 0 : unselected in the monitoring events 1 : selected in the monitoring events
1 (0)	VGA selected (Mem AB region write, I/O 3B0h-3BFh write) 0 : unselected in the monitoring events 1 : selected in the monitoring events
2 (0)	HDD selected (1F0h-1F7h) 0 : unselected in the monitoring events 1 : selected in the monitoring events
3 (0)	IRQ selected 0 : unselected in the monitoring events 1 : selected in the monitoring events
4 (0)	LPT selected (378-37Fh, 278-27Fh, 3BC-3BEh) 0 : unselected in the monitoring events 1 : selected in the monitoring events
5 (0)	COM selected (3F8-3FFh, 2F8-2FFh, 3E8-3EFh, 2E8-2EEH) 0 : unselected in the monitoring events 1 : selected in the monitoring events
6 (0)	FDD selected (3F0-3F7h) 0 : unselected in the monitoring events 1 : selected in the monitoring events
7 (0)	DRQ selected 0 : unselected in the monitoring events 1 : selected in the monitoring events

Detailed Bit Description:

Bit No.	Description
0 - 7	These 8 bits are used to define the system Mode timer monitoring events. The selected active events will reset or clear the Mode idle timer when the respective bit be set to 1. The IRQ group and DRQ group are defined in the Index-36h, 37h(for IRQ) and Index-38h(for DRQ). The VGA address mapping definition is defined in the Index-3Ch bit 0 and bit 1.

Register Name: Mode Timer Monitoring Events Selection Register II
Register Index: 32h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	GP/IO selected 0 : unselected in the monitoring events 1 : selected in the monitoring events
1 (0)	GP/MEM selected 0 : unselected in the monitoring events 1 : selected in the monitoring events
2 (0)	Input_device selected 0 : unselected in the monitoring events 1 : selected in the monitoring events
3 (0)	DRQ events is qualified with DRQ masked registers setting 0 : DRQ be qualified with DMR 1 : DRQ NOT be qualified with DMR
4 (0)	Clock Throttling feature 0 : disable the clock throttling feature 1 : enable the clock throttling feature
5 (0)	IRQ3 selected in the Input_device group 0 : unselected in the Input_device group 1 : selected in the Input_device group
6 (0)	IRQ4 selected in the Input_device group 0 : unselected in the Input_device group 1 : selected in the Input_device group
7 (0)	IRQ12 selected in the Input_device group 0 : unselected in the Input_device group 1 : selected in the Input_device group

Detailed Bit Description:

Bit No.	Description
0 - 2	These 3 bits are used to define the system Mode timer monitoring events. The selected active events will reset or clear the Mode idle timer when the respective bit is set to 1. The GP/IO's definition is defined in the Index-3Ch bit 2~ bit 4. The GP/MEM's definition is defined in the Index 25h, 26h, and 27h. The Input-device group is defined in the Index-32h bit 5~ bit 7.
3	The DRQ group(selected in the Index-38h) will be qualified the M8237 masked registers setting when this bit is set to 0. Otherwise, the DRQ will not qualify masked registers setting.
4	The throttling active STPCLKJ will be unconditionally de-asserted when an SMI or INTR event is issued. i.e. the throttling STPCLKJ de-asserted will not be controlled by the IRQs group (Index-36h and Index-37h). The clock throttling feature can be enabled only when the PMU feature is enabled (i.e. the index-30h D2 should be set to “1” first).
5 - 7	These 3 bits are used to define the Input_device group(or timer) monitoring events. The IRQ1 event is alwaysdefined in the Input_device group. i.e. the IRQ1 active event will always be treated as the Input_device active event. The IRQ3, IRQ4, and IRQ12 active events will be treated as the Input_device active events when their respective bit is set to 1. The Input_device active events will reset/clear the Mode idle timer when the Input_device events is selected in the Mode monitoring events setting(Index-32h bit 2 be set to 1). And, the Input_device active will also reset/clear the Input_device idle timer when this timer is enabled (refer to the Index-3Ah).

Register Name: SMI Triggered Events Selection Register I
Register Index: 33h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	Mode timer time-out event 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
1 (0)	Input_device timer time-out event 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
2 (0)	GP/MEM timer time-out event 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
3 (0)	RTC alarm event 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
4 (0)	Input_device active event 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
5 (0)	IRQ active event 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
6 (0)	DRQ active event 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
7 (0)	EXTSW (suspend switch) active event 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events

Detailed Bit Description:

Bit No.	**Description**
0 - 7	These 7 bits are used to define the SMI events triggered sources. The occurrence of the selected event will issue a SMI active be triggered. The Mode timer is defined in the Index-39h. The Input_device timer is defined in the Index-3Ah. The GP/MEM timer is defined in the Index-3Bh. The RTC alarm event is defined the IRQ8 active event. The Input_device active event is defined in the Index-32h bit 5~ bit 7. The IRQ group is defined in the Index-36h and 37h. The DRQ group is defined in the Index-38h. The EXTSW(suspend switch) is defined in the index-34h bit 5 ~ bit 6.

Register Name: SMI Triggered Events Selection Register II
Register Index: 34h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	VGA access(Write A0000~BFFFFh, port 3B0~3BFh) 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
1 (0)	HDD access (R/W port 1F0~1F7h) 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
2 (0)	LPT access (R/W 378~37Fh or 278~27Fh) 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
3 (0)	GP/IO access (R/W GP/IO defined area) 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
4 (0)	GP/MEM access (R/W GP/MEM defined area) 0 : unselected in the SMI triggered events 1 : selected in the SMI triggered events
5 (0)	EXTSW input low-to-high polarity selected 0 : disable low to high active 1 : enable low to high active
6 (0)	EXTSW input high-to-low polarity selected 0 : disable high to low active 1 : enable high to low active
7 (0)	Double counter time base feature 0 : disable the timer time base be doubled 1 : enable the timer time base be doubled

Detailed Bit Description:

Bit No.	Description
0 - 4	These 5 bits are used to define the accessed events for I/O trap SMI.
5 - 6	These 2 bits are used to define the external switch (suspend button) transition event for SMI event trigger. An external switch low-to-high transition event will issue a SMI request when the bit 5 is set to 1 and the EXTSW is set to trigger the SMI. And, an external switch high-to-low transition event will issue a SMI request. When the bit 6 is set to 1 and the EXTSW is set to trigger the SMI(i.e. the bit 7 of Index-33h is set to 1).
7	All the timer time base of Index-39h, 3Ah, and 3Bh will be doubled when this bit is set to 1.

Register Name: SMI Status Register
Register Index: 35h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 3 (Read-only) (0h)	The cause of the present active SMI event : D3~D0: SMI cause 0000 : NONE 0001 : Mode timer time-out 0010 : Input_device timer time-out 0011 : GP/MEM timer time-out 0100 : RTC alarm 0101 : Input_device active 0110 : IRQ active 0111 : DRQ active 1000 : EXTSW active 1001 : VGA access (W A0000~BFFFFh, port 3B0~ 3BFh) 1010 : HDD access (R/W 1F0~1F7h) 1011 : LPT access (R/W 378~37Fh or 278~27Fh) 1100 : GP/IO access(R/W GP/IO defined area) 1101 : GP/MEM access(R/W GP/MEM defined area) 1110 : Software SMI 1111 : Hardware turbo status transition
4 - 5 (0h)	SMI event trigger signal selected D5D4: SMI signal selected 00 : SMI signal selected 01 : NMI signal selected 10 : IRQ15 signal selected 11 : IRQ10 signal selected
6 - 7 (0h)	SMI signal control selected D7D6: SMI signal control selected 00 : Intel SMI supported 01 : Cyrix SMI supported 10 : AMD SMI supported 11 : reserved

Detailed Bit Description:

Bit No.	Description
0 - 3	These 4 bits are used to describe the triggered cause of the present SMI event.
4 - 5	These 2 bits are used to select the triggered algorithm of the SMI events.
6 - 7	These 2 bits are used to control the SMI signal's timing and polarity for fitting the CPU specification.

Register Name: IRQ Channel Group Selected Control Register I
Register Index: 36h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	IRQ0 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
1	reserved
2 (0)	NMI selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
3 - 4	reserved
5 (0)	IRQ5 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
6 (0)	IRQ6 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
7 (0)	IRQ7 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event

Detailed Bit Description:

Bit No.	Description
0 - 7	These bits are used to define the IRQ channel of the IRQ group. But, the IRQ1, IRQ3, IRQ4, and IRQ12 are not defined in the this group. These 4 IRQs are belong to the Input_device group.

Register Name: IRQ Channel Group Selected Control Register II
Register Index: 37h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	IRQ8 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
1 (0)	IRQ9 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
2 (0)	IRQ10 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
3 (0)	IRQ11 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
4	reserved
5 (0)	IRQ13 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
6 (0)	IRQ14 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event
7 (0)	IRQ15 selected 0 : unselected in the IRQ group event 1 : selected in the IRQ group event

Detailed Bit Description:

Bit No.	Description
0 - 7	These bits are used to define the IRQ channel of the IRQ group. But the IRQ1, IRQ3, IRQ4, and IRQ12 are not defined in this group. These 4 IRQs belong to the Input_device group.

Register Name: DRQ Channel Selected Control Register
Register Index: 38h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (0)	DRQ0 selected 0 : unselected in the DRQ group event 1 : selected in the DRQ group event
1 (0)	DRQ1 selected 0 : unselected in the DRQ group event 1 : selected in the DRQ group event
2 (0)	DRQ2 selected 0 : unselected in the DRQ group event 1 : selected in the DRQ group event
3 (0)	DRQ3 selected 0 : unselected in the DRQ group event 1 : selected in the DRQ group event
4 (0)	PCI Master selected 0 : unselected in the DRQ group event 1 : selected in the DRQ group event
5 (0)	DRQ5 selected 0 : unselected in the DRQ group event 1 : selected in the DRQ group event
6 (0)	DRQ6 selected 0 : unselected in the DRQ group event 1 : selected in the DRQ group event
7 (0)	DRQ7 selected 0 : unselected in the DRQ group event 1 : selected in the DRQ group event

Detailed Bit Description:

Bit No.	Description
0 - 7	These bits are used to define the DRQ channel of the DRQ group.

Register Name: Mode Timer Setting Register
Register Index: 39h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 1 (0h)	Time Base select for Mode timer D1D0 : time base 00 : 1s 01 : 10s 10 : 1min 11 : 10min
2 (0)	Timer count/reset 0 : timer reset 1 : timer starts to count
3 (0)	Timer counter read operation 0 : read the timer counter setting (D7~D4 setting) 1 : read the timer counter current value in D7~D4
4 - 7 (0h)	sets the time-out period of Mode timer 0-15 : time-out count setting Note : timer time-out setting is described as below : Timer timeout set (D7 -6 -5 -4) / Time_base set (1s 10s 1min 10min) 0 0 0 0 — 16s 160s 16min 160min 0 0 0 1 — 1s 10s 1min 10min 0 0 1 0 — 2s 20s 2min 20min 0 0 1 1 — 3s 30s 3min 30min 0 1 0 0 — 4s 40s 4min 40min 0 1 0 1 — 5s 50s 5min 50min 0 1 1 0 — 6s 60s 6min 60min 0 1 1 1 — 7s 70s 7min 70min 1 0 0 0 — 8s 80s 8min 80min 1 0 0 1 — 9s 90s 9min 90min 1 0 1 0 — 10s 100s 10min 100min 1 1 1 1 — 11s 110s 11min 110min 1 1 0 0 — 12s 120s 12min 120min 1 1 0 1 — 13s 130s 13min 130min 1 1 1 0 — 14s 140s 14min 140min 1 1 1 1 — 15s 150s 15min 150min With the setting of the double time based(Index 37h bit_7), the timeout time of the timer will be doubled.

Detailed Bit Description:

Bit No.	Description
0 - 1	These 2 bits are used to set the timeout time base of the timer.
2	The timer counter will be reset/clear when this bit is set to 0. Otherwise, the timer counter will start and keep up-count operation.
3	The bit 7 to bit 4 will be read as the count current value of the timer when this bit is set to 1. Otherwise, the bit 7 to bit 4 will be read as the count setting value of the timer.
4 - 7	These 4 bits are used to set the timeout count value of the timer. These bits are used to define the Mode/Input_device/GP_MEM timer timeout period.

Register Name: Input_device Timer Setting Register
Register Index: 3Ah
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 1 (0h)	Time Base select for Input_device timer D1D0 : time base 00 : 1s 01 : 10s 10 : 1min 11 : 10min
2 (0)	Timer count/reset 0 : timer reset 1 : timer start to count
3 (0)	Timer counter read operation 0 : read the timer counter setting (D7~D4 setting) 1 : read the timer counter current value in D7~D4
4 - 7 (0h)	sets the time-out period of Mode timer 0-15 : time-out count setting Note : timer time-out setting is described as Index 39h.

Detailed Bit Description:

Bit No.	Description
0 - 1	These 2 bits are used to set the timeout time base of the timer.
2	The timer counter will be reset/clear when this bit is set to 0. Otherwise, the timer counter will start and keep to up-count operation.
3	The bit 7 to bit 4 will be read as the count current value of the timer when this bit is set to 1. Otherwise, the bit 7 to bit 4 will be read as the count setting value of the timer.
4 - 7	These 4 bits are used to set the timeout count value of the timer. These bits are used to define the Mode/Input_device/GP_MEM timer timeout period.

Register Name: GP/MEM Timer Setting Register
Register Index: 3Bh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 1 (0h)	Time Base select for GP/MEM timer D1D0 : time base 00 : 1s 01 : 10s 10 : 1min 11 : 10min
2 (0)	Timer count/reset 0 : timer reset 1 : timer start to count
3 (0)	Timer counter read operation 0 : read the timer counter setting (D7~D4 setting) 1 : read the timer counter current value in D7~D4
4 - 7 (0h)	Sets the time-out period of Mode timer 0-15 : time-out count setting

Note: (1)Timer time-out setting is described as Index 39h.
(2)The GP/MEM region are defined in the Index 25h to Index 27h.

Detailed Bit Description:

Bit No.	Description
0 - 1	These 2 bits are used to set the timeout time base of the timer.
2	The timer counter will be reset/clear when this bit is set to 0. Otherwise, the timer counter will start and keep to up-count operation.
3	The bit 7 to bit 4 will be read as the count current value of the timer when this bit be set to 1. Otherwise, the bit 7 to bit 4 will be read as the count setting value of the timer.
4 - 7	These 4 bits are used to set the timeout count value of the timer. These bits are used to define the Mode/Input_device/GP_MEM timer timeout period.

Register Name: LED Flash Control Register
Register Index: 3Ch
Default Value: 03h
Attribute: Read/Write

Bit No.	Bit Function
0 (1)	VGA monitor memory write A0000h-B0000h 0 : Disable the A/B region in VGA group 1 : Enable the A/B region in VGA group
1 (1)	VGA monitor IO write 3B0h-3BFh 0 : Disable the 3Bxh in VGA group 1 : Enable the 3Bxh in VGA group
2 (0)	GP/IO address 100h~1FFh definition 0 : Disable the 1xxh in GP/IO group 1 : Enable the 1xxh in GP/IO group
3 (0)	GP/IO address 200h~2FFh definition 0 : Disable the 2xxh in GP/IO group 1 : Enable the 2xxh in GP/IO group
4 (0)	GP/IO address 300h~3FFh definition 0 : Disable the 3xxh in GP/IO group 1 : Enable the 3xxh in GP/IO group
5 (0)	MODE LED flash feature 0 : disable mode LED flash feature 1 : enable mode LED flash feature(duty :50%)
7 - 6 (0h)	MODE LED frequency setting D7D6 : LED frequency 00 : 1 sec 01 : 4 secs 10 : 8 secs 11 : 16 secs

Detailed Bit Description:

Bit No.	Description
0 - 1	These 2 bits are used to identify the monitoring range of VGA accessed cycles.
2 - 4	These 3 bits are used to identify the monitoring range of GP/IO accessed cycles.
5 - 7	These 3 bits are used to define the Mode LED flash function enabled and flash frequency. The flash duty cycle is be fixed to 50%.

Register Name: Miscellaneous Register I
Register Index: 3Dh
Default Value: 01h
Attribute: Read/Write

Bit No.	Bit Function
0 (1)	ISA I/O address fully decoder feature 0 : disable I/O fully decoder feature 1 : enable I/O fully decoder feature
1 (0)	PMU timer read current value feature 0 : disable timer read current value feature 1 : enable timer read current value feature
2 (0)	SMI routine RSM indicator control 0 : non-SMI cycles 1 : RSM indicator control setting
7 - 3	reserved

Detailed Bit Description:

Bit No.	Description
0	The PMU ISA I/O events address decoded range be defined in address line 15 to line 0 (SA15 - SA0) when this bit is set to 1. Otherwise, the PMU ISA I/O events address decoded range is defined in address line 9 to line 0.
1	All the bit7 to bit4 (D7 - D4) of the PMU timer registers can be read as the current count value when this bit is set to 1. Otherwise, the D7-D4 definition of the PMU timer is defined in the D3 of the respective timer register.
2	In the SMI routine, the software programmer should write a 1 to this bit just before the RSM instruction for indicating the resume from SMI state.
7 - 3	These bits must be kept on 0 for system normal operation.

Register Name: Reserved Register
Register Index: 3Eh
Attribute: Reserved

Register Name: Shadow Port 70h Register
Register Index: 3Fh
Default Value: 00h
Attribute: Read-only

Bit No.	Bit Function
7 - 0	Shadow I/O port for port 70H data

Detailed Bit Description:

Bit No.	Description
7 - 0	These 8 bits are used to record the latest RTCAS - Port 70h data for SMI routine RTC address strobe status restored use.

Register Name: Clock Generator Control Feature Register
Register Index: 40h
Default Value: 03h
Attribute: Read/Write

Bit No.	Bit Function
0 (1)	CLKCTL control signal 0 : set to low or latched trigger event 1 : set to high
1 (R) (1)	CLKCTL signal status 0 : low status 1 : high status
2 (0)	CLKCTL function definition 0 : Green Level indication 1 : Latched CLKCTL signal for PWR control
3 - 4 (0h)	Deturbo function control feature D4D3 : deturbo function control 00 : use CLKCTL for deturbo control 01 : reserved 10 : use CLKCTL for deturbo control 11 : use SMI algorithm for deturbo control
5 (0)	Dummy backoff CPU-bus for deturbo function control 0 : do not use dummy backoff for deturbo function 1 : use dummy backoff for deturbo function
7 - 6 (0h)	reserved

Detailed Bit Description:

Bit No.	Description
0 - 2	These bits are used to define the scheme of the clock generator control in the power-saving mode. When the bit 2 is set to 0, the M1487 will use level sensitive algorithm to control the clock generator operating frequency. i.e. the CLKCTR signal pin will be driven logic "L" when the bit 0 be set to 0, and the CLKCTR will be driven logic "H" when the bit 0 is set to 1. And, the CLKCTR logic state can be read in the bit 1. When the bit 2 is set to 1, the M1487 will use latched triggered algorithm to control the clock generator operating frequency. i.e. the CLKCTR signal pin will be pulsed a Low-transparent/High-latched event to latch the PWR(Index-41h) data from the M1489 pin MA0~MA7 when the bit 0 be writing a 0. And, the bit 0 and bit 1 will automatically return to the logic 1 after the pulsed-latch writing event.
3 - 5	These 2 bits are used to define the algorithm of the deturbo function. When D5 is set to 1 and the bits (D4D3) is set to “01”, the periodical dummy back-off CPU-bus algorithm will be implemented for the deturbo function. And, the dummy back-off time is about 6us of a 8us period in the system side (M1487).
6 - 7	These bits must be kept to "0" for normal operation.

Register Name: Power Control Output Register
Register Index: 41h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 (-)	PWR0 control (MA0 pin of M1489) 0 : set to logic 0 1 : set to logic 1
1 (-)	PWR1 control (MA1 pin of M1489) 0 : set to logic 0 1 : set to logic 1
2 (-)	PWR2 control (MA2 pin of M1489) 0 : set to logic 0 1 : set to logic 1
3 (-)	PWR3 control (MA3 pin of M1489) 0 : set to logic 0 1 : set to logic 1
4 (-)	PWR4 control (MA4 pin of M1489) 0 : set to logic 0 1 : set to logic 1
5 (-)	PWR5 control (MA5 pin of M1489) 0 : set to logic 0 1 : set to logic 1
6 (-)	PWR6 control (MA6 pin of M1489) 0 : set to logic 0 1 : set to logic 1
7 (-)	PWR7 control (MA7 pin of M1489) 0 : set to logic 0 1 : set to logic 1

Detailed Bit Description:

Bit No.	Description
0 - 7	These 8 bits are used to define the latched power control output signals via the MA0~MA7 pins of the M1489.

Register Name: PCI INTx Routing Table Mapping Register I
Register Index: 42h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 3	PCI INT1 to ISA IRQ routine mapping table : D3 D2 D1 D0 : ISA mapping IRQ 0 0 0 0 : Disable 0 0 1 0 : IRQ3 0 1 0 0 : IRQ4 0 1 1 0 : IRQ7 1 0 0 0 : reserved 1 0 1 0 : reserved 1 1 0 0 : reserved 1 1 1 0 : reserved 0 0 0 1 : IRQ9 0 0 1 1 : IRQ10 0 1 0 1 : IRQ5 0 1 1 1 : IRQ6 1 0 0 1 : IRQ11 1 0 1 1 : IRQ12 1 1 0 1 : IRQ14 1 1 1 1 : IRQ15
4 - 7	PCI INT2 to ISA IRQ routine mapping table. The mapping definition is same as INT1.

Detailed Bit Description:

Bit No.	Description
0 - 7	These 8 bits are used to routine PCI INT1 and INT2 to ISA IRQ channels. And, the BIOS programmers should be inhibited to set PCI INTx to the reserved ISA IRQ channels.

Register Name: PCI INTx Routing Table Mapping Register II
Register Index: 43h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 3	PCI INT3 to ISA IRQ routine mapping table. The mapping definition is same as INT1.
4 - 7	PCI INT4 to ISA IRQ routine mapping table. The mapping definition is same as INT1.

Detailed Bit Description:

Bit No.	Description
0 - 7	These 8 bits are used to routine PCI INT3 and INT4 to ISA IRQ channels. And, the BIOS programmers should be inhibited to set PCI INTx to the reserved ISA IRQ channels.

Register Name: PCI INTx Sensitivity Register
Register Index: 44h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
3 - 0 (0h)	The PCI INTx sensitivity definition. The PCI INTx level triggered signal will be transferred to ISA edge triggered when its respective bit is set to 1. Otherwise, the PCI INTX level triggered signal will be passed to ISA level triggered (programmed in port 4D0h and 4D1h) when its respective bit is set to 0. bit 0 : INT1 sensitivity setting for ISA bit 1 : INT2 sensitivity setting for ISA bit 2 : INT3 sensitivity setting for ISA bit 3 : INT4 sensitivity setting for ISA
4 (0)	The arbitrated priority of CPU is the lowest setting 0 : disable the CPU lowest priority 1 : set the CPU arbitrated priority to the lowest
5 (0)	The time slot of CPU is half of PCI_MASTER. 0 : the CPU time-slot be equal to the PCI-masters 1 : the CPU time-slot is half of the PCI-masters
6 (0)	DL(0D0000h~0D7FFFh) region cycle definition 0 : DL region not be on-board ROM region 1 : DL region be on-board ROM region
7 (0)	DH(0D8000h~0DFFFFh) region cycle definition 0 : DH region not be on-board ROM region 1 : DH region be on-board ROM region

Detailed Bit Description:

Bit No.	Description
3 - 0	These 4 bits are used to define the PCI INTx mapped ISA IRQs level/edge triggered sensitivity. The BIOS programmer should to keep the consistency of the mapped ISA sensitivity with the definition of the Port 4D0h and 4D1h.
4	This bit is used to define CPU priority in the arbitrated circuits block. The CPU will be treated to the lowest priority in the bus-ownership arbitrated circuits when this bit is set to 1.
5	This bit is used to define the time slot relation between the CPU and the PCI masters.
6	This bit is used to recognize the on-board ROM with D- lower(0D0000h~0D7FFFh) region feature. When it is set to 1, the D-lower memory region cycle will be treated as the on-board ROM access cycle. And, the ROMCSJ will be asserted in the D-lower region memory assess cycle. Otherwise, the D-lower region memory cycle will be treated as a normal ISA access cycle.
7	This bit is used to recognize the on-board ROM with D-upper(0D8000h~0DFFFFh) region feature. When it is set to 1, the D-upper memory region cycle will be treated as the on-board ROM access cycle. And, the ROMCSJ will be asserted in the D-upper region memory assess cycle. Otherwise, the D-upper region memory cycle will be treated as a normal ISA access cycle.

Note: The M1487 provides two 8-bit R/W registers for supporting ISA edge or level sensitive interrupts on a channel by channel basis. The two registers are 04D0h for master interrupt controller and 04D1h for slave interrupt controller. These registers are used to set the interrupts to be triggered by either the signal edge or the logic level. IRQ0, IRQ1, IRQ2, IRQ8, IRQ13 must be set to edge sensitive for AT traditional usage. After the system reset all IRQ signals are set to edge sensitive. The description below shows which bit numbers represent the various IRQ signal. (0 = edge sensitive; 1 = level sensitive.)

Port 04D0h	(R/W) 00h
D0	IRQ0
D1	IRQ1
D2	IRQ2
D3	IRQ3
D4	IRQ4
D5	IRQ5
D6	IRQ6
D7	IRQ7

Port 04D1h	(R/W) 00h
D0	IRQ8
D1	IRQ9
D2	IRQ10
D3	IRQ11
D4	IRQ12
D5	IRQ13
D6	IRQ14
D7	IRQ15

Register Name: Miscellaneous Register II
Register Index: 45h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
0 - 2	reserved
4 - 3	D4D3 : System reset asserted function control feature during CPU soft reset period. D3 : System reset (SYSRST_pin 63 of M1487) asserted function control during CPU soft-reset period. 0 : SYSRST will not be asserted active (high) during CPU soft reset period. 1 : SYSRST will be asserted active (high) during CPU soft reset period. D4 : System reset (SYSRSTJ_pin 81 of M1487) asserted function control during CPU soft-reset period. 0 : SYSRST will not be asserted active (low) during CPU soft reset period. 1 : SYSRST will be asserted active (low) during CPU soft reset period.
5 (0)	IBC swap MIOJ definition in special cycle 0 : disable swap MIOJ in special cycle 1 : enable swap MIOJ in special cycle (related to Index-12h D5)
6 (0)	Keyboard chip select signal active feature in the fast keyboard emulation cycles. 0 : disable KBCSJ in the fast keyboard emulation cycles. 1 : enable KBCSJ in the fast keyboard emulation cycles.
7 (0)	IOCHRDYJ signal be synchronized by the AT clock in the DMA/ISA master cycles. 0 : IOCHRDYJ will not be sync. by the AT clock in the DMA/ISA master cycles. 1 : IOCHRDYJ will be sync. by the AT clock in the DMA/ISA master cycles.

Detailed Bit Description:

Bit No.	Description
0 - 2	These bits must be kept on 0 for system normal operation.
3 - 4	These 2 bits are used to define the system reset, SYSRST-pin 63 of M1487 and SYSRSTJ-pin 81 of M1487, actve asserted function during the CPU soft-reset period.
5	This bit is used to swap the MIOJ signal in the CPU special cycle decoding. When it be set to 1, the CPU special cycle will be recognized as the Memory-Code-Write access cycle. Otherwise, the CPU special cycle will be recognized as the I/O-Code-Write access cycle. This bit should be programmed in the same definition as the Index-12h D5 for system consistency.
6	This bit is used to enable the keyboard ChipSelect signal be active in the fast keyboard emulation cycles(such as the fast RC or fast gate-A20 cycles) for the consistency between the fast keyboard emulating blocks and the real keyboard ports.
7	This bit is used to enable the synchronized circuits for the IOCHRDYJ in the DMA/ISA master cycles for fitting the timing specification of all ISA master cards.

III. PCI Configuration Cycle Control Ports

(a) Register Name: Configuration Address Register
I/O Address: 0CF8H
Default Value: 00000000h
Attribute: Read/Write
Size: This register must be 32-Bit I/O access in configuration access mechanism #1.

Bit No.	Bit Function
31 (0)	0 : Configuration Disable 1 : Configuration Enable
30-24 (00h)	reserved.
23-16 (00h)	Bus Number. When the bus number is programmed to 00H, the target of the configuration is directly connected to M1489 And a type 0 configuration cycle is generated. If the bus number is non-zero, a type 1 configuration cycle is generated on PCI.
15-11 (00h)	Device Number. It is used by M1489 to drive the IDSEL lines that select a specific PCI device during initialization. The IDSEL lines are only driven when BUS Number is 0h, other the M1489 sends the configuration to a PCI to PCI bridge device.
10-8 (0h)	Function Number. It is used to select a specific device function during initialization.
7-2 (00h)	Register Number. It is used to select a specific register during initialization.
1-0 (0h)	reserved. Fixed at '00'.

(b) Register Name: Configuration Data Register
I/O Address: 0CFCH
Default Value: 00000000h
Attribute: Read/Write
Size: This register may be 8-32-Bit I/O access in configuration access mechanism #1.
Description: This register contains the information which is sent or received during the PCI bus data phase of configuration write or read cycles. CPU access of 8, 16 or 32 bits wide to this register are supported.

(c) Register Name: Configuration Space Enable Register
I/O Address: 0CF8H
Default Value: 00h
Attribute: Read/Write
Size: This register must be 8-Bit I/O access in configuration access mechanism #2.

Bit No.	**Bit Function**
7-4 (0h)	Key Field. When the Key field is programmed to 0H, the PCI configuration space is disabled. When the key field is programmed to a non-zero value, all CPU accesses to CnXXH are forwarded to PCI as configuration space accesses.
3-1 (0h)	Function Number. It is used to select a specific device function during initialization.
0 (0)	reserved. Fixed at '00'.

(d) Register Name: Forward Register
I/O Address: 0CFAH
Default Value: 00h
Attribute: Read/Write
Size: This register must be 8-Bit I/O access in configuration access mechanism #2.

Bit No.	Bit Function
7-0 (00h)	Bus Number. When the bus number is programmed to 00H, the target of the configuration is directly connected to M1489 And a type 0 configuration cycle is generated. If the bus number is non-zero, a type 1 configuration cycle is generated on PCI.

(e) Register Name: PCI Mechanism Control Register
I/O Address: 0CFBH
Default Value: 00h
Attribute: Read/Write
Size: This register must be 8-Bit I/O access in configuration access.

Bit No.	Bit Function
7-1 (0h)	reserved.
0 (0)	PCI Configuration Access Mechanism Select. 0 : Mechanism #2 is selected. 1 : Mechanism #1 is selected.

IV. IDE Controller Related Ports

Configuration I/O Port Address
F4 => ID Port
F8 => Index Port
FC => Data Port
(The ID of M1489 IDE_C is 30H.)

Programming Procedure:
1. Write data to ID port with right ID.
2. Read back data from ID port and check ID. If ID is correct, then IDE_C enter the configuration mode.
3. Program Index, Data to set configuration.
4. IDE_C will remain in configuration mode until write ID port other than its own ID.

Example:

IOW F4H, 30H;
IOR F4H;
IOW F8H, Index;
IOW FCH, Data;
.....
IOW F4H,FFH;

IDE_C Configuration Register.

Register Name: IC_Revision
Register Index: 00h
Default Value: 57h
Attribute: Read only

Register Name: IDE Configuration Register
Register Index: 01h
Default Value: 02h
Attribute: Read/Write

Bit No.	Bit Function
7 (0)	Enable Fast Switch for IDE-1. 0 : Individual I/O command of disk 0 and disk 1 at address 1F0. 1 : Enable the same I/O command of disk 0 and disk 1 at address 1F0 by using the programmed command timing of disk 0.
6-4 (0h)	reserved.
3 (0)	IDE_C Configuration Write Timing. 0 : IDE_C asserts RDYOJ at 2nd T2. 1 : IDE_C asserts RDYOJ at 1st T2.
2 (0)	IDE_C Configuration Read Timing. 0 : IDE_C asserts RDYOJ at 2nd T2. 1 : IDE_C asserts RDYOJ at 1st T2.
1 (1)	IDE_C Assert Data Timing. 0 : IDE_C asserts data after 1st T2. 1 : IDE_C Asserts data at 1st T2.
0 (0)	Enable Disk Operation. 0 : Disable all operation at I/O address. 1 : allow to respond to IDE address 1F0-1F7H, 3F6-3F7H, 170-177H, 376-377H, and enable bridge address range. The reset state of this bit is disabled. BIOS has to enable this bit before IDE access.

Register Name: DBA Data Byte Active Count for IDE-1
Register Index: 02h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-1 3F6,1F1-1F7 IDE 8-Bit command port I/O read/write command active time. D4-D0 access time from 1 to 32 CPU clock, 1 => D4-D0 is "00001" 32 => D4-D0 is "00000".

Register Name: D0RA Disk 0 Read Active Count for IDE-1
Register Index: 03h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-1 disk 0 port 1F0 I/O 16 bits read command active time.

Register Name: D0WA Disk 0 Write Active Count for IDE-1
Register Index: 04h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-1 disk 0 port 1F0 I/O 16 bits write command active time.

Register Name: D1RA Disk 1 Read Active Count for IDE-1
Register Index: 05h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-1 disk 1 port 1F0 I/O 16 bits read command active time.

Register Name: D1WA Disk 1 Write Active Count for IDE-1
Register Index: 06h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-1 disk 1 port 1F0 I/O 16 bits write command active time.

Register Name: Buffer Mode Register 1
Register Index: 07h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7 (0)	Reset Buffer. 0 : Normal buffer action. 1 : Reset buffer. This bit is used to reset buffer when buffer fails.
6 (0)	Enable IDE Write Sector Command. 0 : Disable 1 : Enable When buffer is enabled (D0=1), enabling this bit will make IDE_C to snoop I/O write 1F7 or 177 data. If write data is 30 or 31, IDE_C will enable 1F0 or 170 write cycle to use write post buffer.
5 (0)	Enable IDE Read Sector Command. 0 : Disable 1 : Enable When buffer is enabled (D0=1), enabling this bit will make IDE_C to snoop I/O write 1F7 or 177 data. If write data is 20 or 21, IDE_C will enable 1F0 or 170 read cycle to use read ahead buffer.
4 (0)	Enable IDE Write Buffer Command. 0 : Disable 1 : Enable When buffer is enabled (D0=1), enabling this bit will make IDE_C to snoop I/O write 1F7 or 177 data. If write data is E8, IDE_C will enable 1F0 or 170 write cycle to use write post buffer.
3 (0)	Enable IDE Read Buffer Command. 0 : Disable 1 : Enable When buffer is enabled (D0=1), enabling this bit will make IDE_C to snoop I/O write 1F7 or 177 data. If write data is E4, IDE_C will enable 1F0 or 170 read cycle to use read ahead buffer.
2 (0)	Enable IDE Write Multiple Command. 0 : Disable 1 : Enable When buffer is enabled (D0=1), enabling this bit will make IDE_C to snoop I/O write 1F7 or 177 data. If write data is C5, IDE_C will enable 1F0 or 170 write cycle to use write post buffer.
1 (0)	Enable IDE Read Multiple Command. 0 : Disable 1 : Enable When buffer is enabled (D0=1), enabling this bit will make IDE_C to snoop I/O write 1F7 or 177 data. If write data is C4, IDE_C will enable 1F0 or 170 read cycle to use read ahead buffer.
0 (0)	Enable IDE Read/Write Buffer. 0 : Disable 1 : Enable This bit is used to enable/disable IDE read ahead buffer and IDE write post buffer.

Register Name: IDEPE IDE Port Enable Register
Register Index: 08h
Default Value: FFh
Attribute: Read only

Bit No.	Bit Function
7-0 (FFh)	It is used to define 1F7-1F0 address will be decoded or not, it means that register is set to one, the address belongs to IDE.

Register Name: IDEPE1 IDE Port Enable Register1
Register Index: 09h
Default Value: 41h
Attribute: Read/Write

Bit No.	Bit Function
7-6 (1h)	Define Internal Delay ADSJ. 00 : No delay. 01 : Delay ADSJ 1 clock. 10 : Delay ADSJ 2 clock. 11 : Delay ADSJ 2 clock.
5-2 (0h)	reserved.
1 (0)	It is used to define 3F7 address will be decoded or not. 0 : Not belonged. 1 : Belonged.
0 (1)	It is used to define 3F6 address will be decoded or not. 0 : Not belonged. 1 : Belonged.

Register Name: Buffer Mode Register 2
Register Index: 0Ah
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7(0)	reserved
6 (0)	Enable IDE CD ROM Command. 0 : Disable 1 : Enable When buffer is enabled (index-07h D0=1), enabling this bit will make IDE_C to snoop I/O write 1F7 or 177 data and I/O write 1F0 or 170 data port and I/O read 1F7 or 177. If write 1F7 or 177 Data is A0 and write 1F0 or 170 data is 28 or A8, read ahead buffer will be enabled after I/O read 1F7 or 177.
5-4(0h)	reserved.
3 (0)	Enable IDE Channel 2 Disk 1 Buffer. 0 : Disable 1 : Enable When buffer is enabled (index-07H D0=1), enable this bit will enable IDE channel 2 disk 1 data access to use read ahead buffer and write post buffer.
2 (0)	Enable IDE Channel 2 Disk 0 Buffer. 0 : Disable 1 : Enable When buffer is enabled (index-07H D0=1), enabling this bit will enable IDE channel 2 disk 0 data access to use read ahead buffer and write post buffer.
1 (0)	Enable IDE Channel 1 Disk 1 Buffer. 0 : Disable 1 : Enable When buffer is enabled (index-07H D0=1), enabling this bit will enable IDE channel 1 disk 1 data access to use read ahead buffer and write post buffer.
0 (0)	Enable IDE Channel 1 Disk 0 Buffer. 0 : Disable 1 : Enable When buffer is enabled (index-07H D0=1), enabling this bit will enable IDE channel 1 disk 0 data access to use read ahead buffer and write post buffer.

Register Name: IDE Channel 1 Disk 0 Sector Byte Count Register 1
Register Index: 0Bh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-2 (00h)	Sector Byte Count [7:2].
1-0	Sector Byte Count [1:0], Always Set to Be 0. (0h)

Register Name: IDE Channel 1 Disk 0 Sector Byte Count Register 2
Register Index: 0Ch
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (00h)	reserved.
4-0 (2h)	Sector Byte Count [12:8], Sector Byte Count [12:0] is used to defined how many bytes are in a sector. In AT environment, it is 512 bytes.

Register Name: IDE Channel 1 Disk 1 Sector Byte Count Register 1
Register Index: 0Dh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-2 (00h)	Sector Byte Count [7:2].
1-0 (0h)	Sector Byte Count [1:0], always set to be 0.

Register Name: IDE Channel 1 Disk 1 Sector Byte Count Register 2
Register Index: 0Eh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (00h)	reserved.
4-0 (2h)	Sector Byte Count [12:8], Sector Byte Count [12:0] is used to defined how many bytes are in a sector. In AT environment, it is 512 bytes.

Register Name: IDE Channel 2 Disk 0 Sector Byte Count Register 1
Register Index: 0Fh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-2 (00h)	Sector Byte Count [7:2].
1-0 (0h)	Sector Byte Count [1:0], always set to be 0.

Register Name: IDE Channel 2 Disk 0 Sector Byte Count Register 2
Register Index: 10h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (00h)	reserved.
4-0 (2h)	Sector Byte Count [12:8], Sector Byte Count [12:0] is used to defined how many bytes are in a sector. In AT environment, it is 512 bytes.

Register Name: IDE Channel 2 Disk 1 Sector Byte Count Register 1
Register Index: 11h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-2 (00h)	Sector Byte Count [7:2].
1-0 (0h)	Sector Byte Count [1:0], Always Set to Be 0.

Register Name: IDE Channel 2 Disk 1 Sector Byte Count Register 2
Register Index: 12h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (00h)	reserved.
4-0 (2h)	Sector Byte Count [12:8], Sector Byte Count [12:0] is used to define how many bytes are in a sector. In AT environment, it is 512 bytes.

Register Name: DBR Data Byte Recovery Count for IDE-1
Register Index: 25h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved
4-0 (00h)	used to define IDE-1 3F6,1F1-1F7 IDE 8-Bit command port I/O read/write command recovery time. D4-D0 access time from 1 to 32 CPU clock, 1 => D4-D0 is "00001" 32 => D4-D0 is "00000".

Register Name: D0RR Disk 0 Read Recovery Count for IDE-1
Register Index: 26h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	used to define IDE-1 disk 0 port 1F0 I/O 16 bits read command recovery time.

Register Name: D0WR Disk 0 Write Recovery Count for IDE-1
Register Index: 27h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	used to define IDE-1 disk 0 port 1F0 I/O 16 bits write command recovery time.

Register Name: D1RR Disk 1 Read Recovery Count for IDE-1
Register Index: 28h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	used to define IDE-1 disk 1 port 1F0 I/O 16 bits read command recovery time.

Register Name: D1WR Disk 1 Write Recovery Count for IDE-1
Register Index: 29h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-1 disk 1 port 1F0 I/O 16 bits write command recovery time.

Register Name: DBA Data Byte Active Count for IDE-2
Register Index: 2Ah
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 376,171-177 IDE 8-Bit command port I/O read/write command active time. D4-D0 access time from 1 to 32 CPU clock, 1 => D4-D0 is "00001" 32 => D4-D0 is "00000".

Register Name: D0RA Disk 0 Read Active Count for IDE-2
Register Index: 2Bh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 disk 0 port 170 I/O 16 bits read command active time.

Register Name: D0WA Disk 0 Write Active Count for IDE-2
Register Index: 2Ch
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 disk 0 port 170 I/O 16 bits write command active time.

Register Name: D1RA Disk 1 Read Active Count for IDE-2
Register Index: 2Dh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 disk 1 port 170 I/O 16 bits read command active time.

Register Name: D1WA Disk 1 Write Active Count for IDE-1
Register Index: 2Eh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 disk 1 port 170 I/O 16 bits write command active time.

Register Name: DBR Data Byte Recovery Count for IDE-2
Register Index: 2Fh
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 376,171-177 IDE 8-Bit command port I/O read/write command recovery time. D4-D0 access time from 1 to 32 CPU clock, 1 => D4-D0 is "00001" 32 => D4-D0 is "00000".

Register Name: D0RR Disk 0 Read Recovery Count for IDE-2
Register Index: 30h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 disk 0 port 170 I/O 16 bits read command recovery time.

Register Name: D0WR Disk 0 Write Recovery Count for IDE-2
Register Index: 31h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 disk 0 port 170 I/O 16 bits write command recovery time.

Register Name: D1RR Disk 1 Read Recovery Count for IDE-2
Register Index: 32h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 disk 1 port 170 I/O 16 bits read command recovery time.

Register Name: D1WR Disk 1 Write Recovery Count for IDE-2
Register Index: 33h
Default Value: 00h
Attribute: Read/Write

Bit No.	Bit Function
7-5 (0h)	reserved.
4-0 (00h)	Used to define IDE-2 disk 1 port 170 I/O 16 bits write command recovery time.

Register Name: IDEPE2 IDE Port Enable Register2
Register Index: 34h
Default Value: FFh
Attribute: Read only

Bit No.	Bit Function
7-0 (FFh)	It is used to define 177-170 address will be decoded or not, it means that register is set to one, the address belongs to IDE.

Register Name: IDEPE3 IDE Port Enable Register3
Register Index: 35h
Default Value: 01h
Attribute: Read/Write

Bit No.	Bit Function
7 (0h)	Enable Fast Switch for IDE-2. 0 : Individual I/O command of disk 0 and disk 1 at address 170. 1 : Enable the same I/O command of disk 0 and disk 1 at address 170 by using the programmed command timing of Disk 0.
6 (0h)	RAID1(Disk Mirror) Enable/Disable. 0 : Disable 1 : Enable
5 (0h)	RAID1(Disk Mirror) Read Enable/Disable. 0 : Disable 1 : Enable
4 (0h)	RAID1(Disk Mirror) Write Enable/Disable. 0 : Disable 1 : Enable
3 (0h)	RAID0 Enable/Disable. 0 : Disable 1 : Enable
2 (0h)	Define ODD/EVEN in RAID0 Enable Mode. 0 : Even. 1 : Odd. When this bit is programmed to be Even, it will drive HD[15-0]. When this bit is programmed to be Odd, it will drive HD[31-16].
1 (0h)	Define 377 Belong to IDE Or Not. 0 : Not belong 1 : Belong
0 (1h)	Define 376 Belong to IDE Or Not. 0 : Not belonged. 1 : Belonged.

V. PCI Configuration Space:

M1489 will respond to CPU/PCI configuration access for which AD16 is high in address cycle.

Register Name: VID - Vendor Identification Register
Register Index: 01, 00h
Default Value: 10B9h
Attribute: Read only
Size: 16 bits
Description: This is a 16 bits value assigned to Acer Labs Inc. This register is combined with 03h-02h uniquely identify any PCI device. Write to this register has no effect.

Register Name: DID - Device Identification Register
Register Index: 03,02h
Default Value: 1489h
Attribute: Read only
Size: 16 bits
Description: This is a 16 bit value assigned to M1489.

Register Name: COM - Command Register
Register Index: 05,04h
Default Value: 0007h
Attribute: Read/Write
Size: 16 bits

Bit No.	Bit Function
15-7 (000h)	reserved.
6(0)	Respond to Parity Errors Enable/Disable. 0 : Disable 1 : Enable When this bit is set, M1489 will generate PERRJ if a parity error is detected. When this bit is reset, M1489 will ignore any parity errors that it detects.
5(0)	Enable VGA Palette Snooping. M1489 does not support this. Write to this bit has no effect.
4(0)	Enable Postable Memory Write Command. M1489 does not support. Write to this bit has no effect.
3(0)	Enable Special Cycle. M1489 does not support this. Write to this bit has no effect.
2(1)	Control to Act As a PCI Bus Master. M1489 does not support to disable bus master operations. This bit is set to 1 on Power-On to enable PCI master operations. Write to this bit has no effect.
1(1)	Enable Response to Memory Access. M1489 always accepts PCI master accesses to DRAM.
0(1)	Enable Response to I/O Access. M1489 always accepts PCI master accesses to ISA I/O Space.

Register Name: DS - Device Status Register
Register Index: 07,06h
Default Value: 0400h
Attribute: Read/Write
Size: 16 bits

Bit No.	Bit Function
15(0)	Parity Error. This bit is set by the device whenever it detects a parity error in a PCI transaction even if parity error handling is disabled (As control by bit6 in the command register).
14(0)	reserved. M1489 does not assert SERRJ.
13(0)	Master Abort. This bit is set by M1489 whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.
12(0)	Received Target Abort. This bit is set by M1489 whenever its initiated transaction is terminated with a target abort. This bit is cleared by writing a 1 to it.
11(0)	Sent Target Abort. This bit is set by devices that whenever acting as a target terminate a transaction by target abort. M1489 never terminates a transaction with target abort therefore this bit is never set. Write to this bit has no effect.
10-9 (10)	DEVSELJ Timing. 00 : Fast 01 : Medium 10 : Slow M1489 timing for DEVSELJ assertion. Slow timing is selected.
8-0 (000h)	reserved.

Register Name: RI - Revision ID Register
Register Index: 08h
Default Value: 00h
Attribute: Read only
Size: 8 bits

Register Name: CC - Class Code Register
Register Index: 0B,0A,09h
Default Value: 060000h
Attribute: Read only
Size: 24 bits

Register Name: Reserved Register
Register Index: FF-0Ch
Default Value: 00000000h
Attribute: Read only

VI. ISA Compatible Registers Summary:

The ISA compatible registers of M1489/M1487 are summarized as below:

I/O Address	Attribute	Register Name
0000h	Read/Write	DMA1(slave) CH0 Base and Current Address
0001h	Read/Write	DMA1(slave) CH0 Base and Current Count
0002h	Read/Write	DMA1(slave) CH1 Base and Current Address
0003h	Read/Write	DMA1(slave) CH1 Base and Current Count
0004h	Read/Write	DMA1(slave) CH2 Base and Current Address
0005h	Read/Write	DMA1(slave) CH2 Base and Current Count
0006h	Read/Write	DMA1(slave) CH3 Base and Current Address
0007h	Read/Write	DMA1(slave) CH3 Base and Current Count
0008h	Read/Write	DMA1(slave) Status(R)/Command(W)
0009h	Write-only	DMA1(slave) Write Request
000Ah	Write-only	DMA1(slave) Write Single Mask Bit
000Bh	Write-only	DMA1(slave) Write Mode
000Ch	Write-only	DMA1(slave) Clear Byte Pointer
000Dh	Write-only	DMA1(slave) Master Clear
000Eh	Write-only	DMA1(slave) Clear Mask
000Fh	Read/Write	DMA1(slave) Read/Write All Mask Register Bits
0020h	Read/Write	INT_1(master) Control Register
0021h	Read/Write	INT_1(master) Mask Register
0040h	Read/Write	Timer Counter - Channel 0 Count
0041h	Read/Write	Timer Counter - Channel 1 Count
0042h	Read/Write	Timer Counter - Channel 2 Count
0043h	Read/Write	Timer Counter Command Mode Register
0060h	Read_access	Clear IRQ12(for PS2), IRQ1 Latched Status
0060h	Read/Write	Keyboard Data Buffer
0061h	Read/Write	NMI and Speaker Status and Control
0064h	Read/Write	Keyboard Status(R)/Command(W)
0070h	Write-only	CMOS RAM Address Port and NMI Mask Register
0071h	Read/Write	CMOS Data Register Port
0081h	Read/Write	DMA Channel 2 Page Register
0082h	Read/Write	DMA Channel 3 Page Register
0083h	Read/Write	DMA Channel 1 Page Register
0087h	Read/Write	DMA Channel 0 Page Register
0089h	Read/Write	DMA Channel 6 Page Register
008Ah	Read/Write	DMA Channel 7 Page Register
008Bh	Read/Write	DMA Channel 5 Page Register
008Fh	Read/Write	Refresh Address Register for Address 23 to 17

00A0h	Read/Write	INT_2(slave) Control Register
00A1h	Read/Write	INT_2(slave) Mask Register
00C0h	Read/Write	DMA2(master) CH0 Base and Current Address
00C2h	Read/Write	DMA2(master) CH0 Base and Current Count
00C4h	Read/Write	DMA2(master) CH1 Base and Current Address
00C6h	Read/Write	DMA2(master) CH1 Base and Current Count
00C8h	Read/Write	DMA2(master) CH2 Base and Current Address
00CAh	Read/Write	DMA2(master) CH2 Base and Current Count
00CCh	Read/Write	DMA2(master) CH3 Base and Current Address
00CEh	Read/Write	DMA2(master) CH3 Base and Current Count
00D0h	Read/Write	DMA2(master) Status(R)/Command(W)
00D2h	Write-only	DMA2(master) Write Request
00D4h	Write-only	DMA2(master) Write Single Mask Bit
00D6h	Write-only	DMA2(master) Write Mode
00D8h	Write-only	DMA2(master) Clear Byte Pointer
00DAh	Write-only	DMA2(master) Master Clear
00DCh	Write-only	DMA2(master) Clear Mask
00DEh	Read/Write	DMA2(master) Read/Write All Mask Register Bits
00F0h	Write-only	Coprocessor Error Ignored Register
04D0h	Read/Write	INT_1(master) Edge/Level Control
04D1h	Read/Write	INT_2(slave) Edge/Level Control

Section 5: M1489/M1487 Software Programming Guide

5.1 Memory Controller Programming Reference Manual

1. System Memory Programming

(a) Memory configuration of each bank:

Bit3-2-1-0	DRAM Size	DRAM Type
1 1 1 1	None	None
0 0 0 0	1 M	256Kx1
0 0 0 1	4 M	1Mx1
0 0 1 0	2 M	512Kx8
0 0 1 1	16 M	4Mx1
0 1 0 0	64 M	16Mx1
0 1 0 1	8 M	2Mx8(11-10)
0 1 1 0	16 M	4Mx4(12-10)
0 1 1 1	8 M	2Mx8(12-9)
1 0 0 0	4 M	1Mx16(12-8)
(else)	reserved	reserved

Note: 1. "DRAM Size" means the total memory size of the bank.
2. "DRAM Type" "AxB(C-D)" means the DRAM module element is A by B and the number of address mapping is C in row and D in column.
3. The setting "1111" means this bank memory is ignored (disabled).

DRAM configuration of bank 0 : Index-10h D3~D0
DRAM configuration of bank 1 : Index-10h D7~D4
DRAM configuration of bank 2 : Index-11h D3~D0
DRAM configuration of bank 3 : Index-11h D7~D4

The M1489 DRAM configuration of each bank is independent of each other. So, the memory configuration can be programmed in any combination of each bank. In addition, the maximum memory range recognized by M1489/M1487 is 128M, i.e. 00000000h ~ 07FFFFFFh. Please refer to FIG. "MA TABLE" for details.

(b) Shadow region definition:

Shadow region is defined in Index-13h D7~D0, Index-14h D3~D0 and the configuration is shown as below :

(i) definition ==>

Address region	Definition bit
000C0000 ~ 000C3FFF	Index-13h D0
000C4000 ~ 000C7FFF	Index-13h D1
000C8000 ~ 000CCFFF	Index-13h D2
000CD000 ~ 000CFFFF	Index-13h D3
000D0000 ~ 000D3FFF	Index-13h D4
000D4000 ~ 000D7FFF	Index-13h D5
000D8000 ~ 000DCFFF	Index-13h D6
000DD000 ~ 000DFFFF	Index-13h D7
000E0000 ~ 000E7FFF	Index-14h D0
000E8000 ~ 000EFFFF	Index-14h D1
000F0000 ~ 000F7FFF	Index-14h D2
000F8000 ~ 000FFFFF	Index-14h D3

(ii) Setting ==>

Set	region shadow ?
1	Shadow
0	Non-shadow

Shadow region read control:
When Index-14h D4 is set to "1", a shadow region read cycle will be treated as a local memory access cycle, otherwise, an ISA memory access cycle.

Shadow region write control:
When Index-14h D5 be set to "1", a shadow region write cycle will be treated as a local memory access cycle, otherwise, an ISA memory access cycle.

(c) 00F00000 ~ 00FFFFFF (15M) memory space control :

15M range memory space control bit is in Index-12h D3. When Index-12h D3 = "1", the M1489 on-board memory decoder will be forced to recognize the 15M region as ISA memory range. Otherwise, when Index-12h D3 = "0", the M1489 on-board memory decoder will operate in normal condition.

(d) System ROM region definition:
The following table describes the XBUSCSJ/ ROMCSJ (ROM chip select) signal active mapping address region. It is equivalently the definition of the on-board ISA memory region.

Address region	Definition Bit
(*)8FFF0000 ~ FFFFFFFF	Index-21h D5
(**)000F0000 ~ 000FFFFF	--
000E0000 ~ 000EFFFF	Index-12h D0
000D8000 ~ 000DFFFF	Index-44h D7
000D0000 ~ 000D7FFF	Index-44h D6
000C0000 ~ 000C7FFF	Index-12h D2
000C8000 ~ 000CFFFF	Index-12h D1

Note: (*): M1489/M1487 will not recognize the A27 ~A30 signals

(**): M1489/M1487 will recognize 000F0000 ~ 000FFFFF region as on-board ROM region. Setting to "1" means M1487 XBUSCSJ/ ROMCSJ will be activated. Setting to "0" means M1487 XBUSCSJ/ROMCSJ will NOT be activated

(e) Flash ROM R/W support : (Index-12h D4)

It is the normal case that M1489/M1487 will not assert XBUSCSJ/ ROMCSJ when on-board ISA memory write cycles. But if Index-12h D4 is set to be "1", which is "0" by default, the M1489/M1487 will assert XBUSCSJ/ ROMCSJ for not only the on-board ISA memory read, but also the on-board ISA memory write. This feature is used to support the Flash ROM. The on-board ISA memory region is defined as described in the previous section "System ROM region definition".

(f) SMM RAM control
The M1489 supports three different SMM regions. They are AB region, E region and 38000 (68000 for AMD) region. The programming procedure is detailed in the PMU section.

2. DRAM Control

(a) DRAM type & size control:
M1489/M1487 supports 4 banks of DRAM. The maximum local memory range is 128M, i.e. 00000000h ~ 07FFFFFFh. DRAM type and programming is described in previous section (1-a).

(b) Refresh control:
Hidden refresh control bit is in Index-12h D7.
When Index-12h D7 = "0", hidden refresh feature is disable.
When Index-12h D7 = "1", hidden refresh feature is enable.

Refresh period setting bits of normal refresh are in Index-2Ah D6~D5.

Index-2Ah D6 D5	refresh period (of normal refresh)
0 0	15 us
0 1	30 us
1 0	60 us
1 1	120 us

Refresh period setting bits of hidden refresh are in Index-1Ah D7~D6.

Index-1Ah D7 D6	refresh period (of hidden refresh)
0 0	15 us
0 1	30 us
1 0	60 us
1 1	120 us

It is suggested that in power-saving mode, if DRAM hidden refresh is enabled, the DRAM hidden refresh period should be programmed as 15us (Index-1Ah D7D6="00").

(c) RAS active timeout check control:
RAS active timeout check control bit is in Index-12h D6.
When Index-12h D6 = "0", timeout check feature is disable.
When Index-12h D6 = "1", timeout check feature is enable.

(d) DRAM access timing:
The DRAM access timing are defined in Index-1Bh D3~D0. The following two tables list the Standard DRAM read/write access cycle timing:

DRAM Read Timing:

D3 D2 (index1Bh)	Read page miss	Read page hit	Burst Read
0 0 (slow)	CP+11	CP+4	5-5-5
0 1 (normal)	CP+8	CP+3	4-4-4
1 0 (fast)	CP+6	CP+2	3-3-3
1 1 (fastest)	CP+5	CP+1	2-2-2

DRAM Write Timing:

D3 D2 (index1Bh)	Write page miss	Write page hit	Burst Write
0 0 (slow)	CP+8	CP+5	5-5-5
0 1 (normal)	CP+6	CP+4	4-4-4
1 0 (fast)	CP+5	CP+3	3-3-3
1 1 (fastest)	CP+5	CP+3	2-2-2

Note : CP means the Check_Point time

(e) EDO (Extended Data Output) DRAM programming
M1489/ M1487 support EDO type DRAM. The MA table and sizing procedure are the same as normal fast page mode DRAM. Meanwhile, EDO detection and timing programming are detailed as below:

i) Definition of EDO bank:
M1489/M1487 support EDO and standard fast page mode DRAM independently. BIOS could program the 4 banks DRAM as any combination of EDO and fast page mode DRAM. The EDO definition bits for each bank are in Index1Ah

D3~D0. They are described in table below:

DRAM Bank	Definition Bit
0	Index-1Ah D0
1	Index-1Ah D1
2	Index-1Ah D2
3	Index-1Ah D3

setting: '0' => normal fast page mode DRAM
'1' => EDO mode DRAM supported

ii) Detection of EDO:
M1489/M1487 support EDO test mode to distinguish EDO DRAM from standard fast page mode DRAM. The EDO test mode definition bit is in Index-1Ah D5.

When Index-1Ah D5='0' the DRAM controller is operating at normal mode. When Index-1Ah D5='1' the DRAM controller is operating at EDO test mode.

The suggested EDO detection procedure is as following :

Testing pattern TP = 55AA00FFh or other pattern useful
Testing address TA = 00000000h or other address smaller than bank size
For each bank i = 0~3
1. DRAM sizing
2. Set bank i as EDO bank (Index-1Ah D3~D0)
3. Enable EDO test mode (Index-1Ah D5)
4. Write testing pattern TP to address TA
5. TD1 = Read address TA
6. If TD1=TP then this bank is EDO bank, else this bank is not EDO bank; disable bank i as non-EDO bank (Index-1Ah D3~D0)
7. next bank

EDO test mode of M1489/M1487 is supported only when cache (L1 & L2) is disabled. This limitation should be noticed.

iii) EDO timing program :
The timing definition bits of EDO DRAM are the same as standard DRAMs, which are defined in Index 1Bh D3~D0. M1489/M1487 memory controller will respond EDO timing according to EDO bank definition (Index-1Ah D3~D0) for each bank.
Generally speaking, the EDO read timing is shorter than standard DRAM read timing by 1 CPUCLK and the EDO write timing is the same as standard DRAM write timing. But as an exception, when DRAM write timing is programmed as "fastest" (Index-1Bh D3D2 = "11") and "EDO write 2-1-1-1" is enabled (Index-1Ah D4='1'), the EDO write cycle will be finished in 1 CPUCLK for each data. The following two tables list the EDO DRAM read/write access cycle timing:

EDO DRAM Read Timing:

D1 D0 (index1Bh)	Read page miss	Read page hit	Burst Read
0 0 (slow)	CP+11	CP+4	4-4-4
0 1 (normal)	CP+8	CP+3	3-3-3
1 0 (fast)	CP+6	CP+2	2-2-2
1 1 (fastest)	CP+5	CP+1	1-1-1

EDO DRAM Write Timing:

D3 D2 (index1Bh)	Write page miss	Write page hit	Burst Write
0 0 (slow)	CP+8	CP+5	5-5-5
0 1 (normal)	CP+6	CP+4	4-4-4
1 0 (fast)	CP+5	CP+3	3-3-3
1 1 (fastest)	CP+4	CP+2	2-2-2
*1 1 (fastest)	CP+4	CP+1	1-1-1

Note: 1. CP means the Check_Point time
2. * Index-12h D4='1'
3. System Cache programming

(a) Enable level 1 CPU internal cache (L1) and level 2 system cache (L2):

Cache level	Definition Bit
Level 1	Index-16h D0
Level 2	Index-16h D1

The system BIOS should set Index-16h D0 to '1' to signal M1489 that L1 cache in host CPU is enabled. The system BIOS could also set Index-16h D1 to '1' to enable L2 cache operation.

(b) The L1 & L2 cache coherency control:
(i) L1 cache WB/WT option =>
Index-16h D2 :
'0' L1 write-through;
'1' L1 write-back.
(ii) L2 Tag bits option =>
Index-16h D3 :
'0' 7-bits Tag and 1-bit Dirty bit
'1' 8-bits Tag (and force dirty)

Index-16h D2 is used to inform M1489/M1487 that CPU internal cache is write-through or write-back type cache. This is used for M1489/M1487 cache controller to maintain coherency between L1 cache and system memory. M1489/M1487 support write-back L2 cache only. But in order to increase cacheable region, M1489/M1487 support 8bit TAG(Index-16h D3='1') with "Dirty bit" = '1', i.e. force dirty. It is suggested that Index-16h D3 should be programmed before L2 cache sizing.

(c) The L2 cache size configuration
(i) L2 cache SRAM type setting =>
Index-17h D1D0 : '01' 32K*8 SRAM
'10' 64K*8 SRAM
'11' 128K*8 SRAM
(ii) L2 cache structure =>
Index-17h D2 : '0' 1 bank cache; '1' 2 bank cache.
These two configuration together determine the TAG data of cache lines. Please refer to Cache Mapping Table for further details.

(d) L2 cache operation control options:
(i) Force L2 cache miss feature =>
Index-17h D3 : '0' normal operation
'1' force L2 cache miss
This feature is set to force L2 cache 'miss' for either read-cycles or write-cycles.
(ii) Force L2 cache non-dirty feature =>
Index-17h D4 : '0' normal operation
'1' force L2 cache to be non-dirty for read-cycles. This feature is used to force the L2 cache to be non-dirty for read-cycles.
(iii) Force L2 cache hit feature =>
Index-17h D5 : '0' normal operation '1' force L2 cache hit. This feature is set to force L2 cache 'hit' for either read-cycles or write-cycles.

(e) Shadow region cacheability control:

L2 cacheability for the shadow region	Index-17h D6
L1 cacheability for the shadow region	Index-17h D7

Setting : '0' disable cacheability
'1' enable cacheability
This feature controls the cacheability of the data/ code of shadow regions for L1/L2 cache.

(e) L2 Cache timing control
(i) L2 cache read/write timing setting =>
Index-16h D4 : '0' fast L2-write timing;
'1' normal L2-write timing
Index-16h D5 : '0' fast L2-read timing;
'1' normal L2-read timing
When the normal timing is selected, there will be a wait cycle inserted.
(ii) L2 cache write-pulse rising edge option =>
Index-16h D6 : '0' normal XCWEJ timing; '1' fast rising of XCWEJ L2 TAG write-pulse rising edge option =>
Index-16h D7 : '0' normal XTAGWEJ timing;
'1' fast rising of XTAGWEJ
These features above are devoted to avoid the hold-time violation of data and address for the cache and tag SRAMs. For each write-pulse.

4. System Timing Control:

(a) CPU Cycle check point options:
The cycle check point is the memory decoding and hit/miss check time of M1489 in the CPU cycle. This feature is equally to insert wait states in order to increase the time for decoding the cycle commands. The wait state inserted and cycle timing are shown as below.

Register	Check Point	Cycle check Timing	Wait states
Index-15h D5D4: 00	fastest	T1 end	0 wait
Index-15h D5D4: 01	fast	1st T2 end	1 wait
Index-15h D5D4: 10	normal	2nd T2 end	2 wait
Index-15h D5D4: 11	reserved	---	---

(b) Master Cycle check point options:
The cycle check point is the memory decoding and hit/miss check time of M1489 in the Master cycle. This feature is equally to insert wait states in order to increase the time for decoding the cycle commands. The wait state inserted and cycle timing are shown as below.

Register	Check Point	Cycle check Timing	Wait States
Index-15h D7D6: 00	fastest	T1 end	0 wait
Index-15h D7D6: 01	fast	1st T2 end	1 wait
Index-15h D7D6: 10	normal	2nd T2 end	2 wait
Index-15h D7D6: 11	reserved	---	---

(c) Insert 1 wait for Decoding/Checking time option:
The "Insert Wait for Decoding/Checking" feature will delay the M1489 internal cycle start time by 1 CPU-Clock.
Index-29h D1 : '0' normal operation
'1' Insert 1 wait for internal decoding/checking
This feature prevents the M1489 from suffering the setup time violation of ADSJ command or cycle decoding by inserting ONE wait state.

(d) Write-back CPU check timing control:

The CPU HITMJ sampling time after an issued EADSJ snoop signal is defined in Index-19h D2. When D2="0", the HITMJ will be sampled after an issued EADSJ by 2 CPUCLK period. When D2="1", the HITMJ will be sampled after an issued EADSJ by 3 CPUCLK period.

II. PCI Local Bus Controller Programming Reference Manual

5. M1489 CPU to PCI write buffer programming

(a) Fast Dynamic ISA definition:

Fast dynamic ISA feature is unique for ALI chipset. This feature is used to minimize the cycles needed to pass check point of PCI bus. Since the cycle will issue to PCI bus first if it is not a local memory cycle, this cycle will pass to ISA when no PCI device claims this cycle by asserting DEVSELJ. So, it will waste time to wait PCI bus passing DEVSEL# check point (defined by Index-21H Bit 1-0). Fast dynamic ISA feature can be enabled by setting Index-20H bit 0 to 1. M1489 will intelligently memorize the address and command issued to ISA. If the consecutive memory cycles issued by CPU to ISA and the address range within 1K, the second cycle will issue to ISA directlly.

(b) Fast Dynamic PCI definition:

Fast dynamic PCI feature is unique for ALI chipset. This feature is used to remove the need of PCI memory hole. For all PCI chipset implementation, it will define PCI memory holes to utilize CPU to PCI write buffer. The memory address within PCI memory hole can post to write buffer and boost the performance. The most popular memory slave in PCI is VGA card. So, the AT standard A,B segment for VGA can be easily defined(Index-20H bit 7-6). But in frame buffer application, it is very hard to define PCI memory hole for frame buffer.
Fast dynamic PCI feature(Index-20H bit 1) is used to solve this problem. This feature is like fast dynamic ISA feature. M1489 will intelligently memorize the address and command issued to PCI. If the consecutive memory cycles issued by CPU to PCI and the address range within 1K, the second cycle will post to write buffer and boost the performance.

(c) CPU to PCI Write Buffer:

M1489 implements 4-layer double word CPU to PCI Write Buffer. This buffer can be enabled by setting Index-20H bit 2 to 1. It only buffers memory write cycle to PCI bus. It will not serve any I/O cycle until the write buffer is empty. That means if chipset is doing memory write cycle through write buffer and then CPU issues an I/O cycle this cycle has to wait until write buffer has been flushed. It won't buffer and merge any CPU I/O cycle.

(d) CPU to PCI Write Buffer Byte Merge:

This feature is used to merge byte or word to double word, since PCI is a 32-bit bus. It is very useful in not 32-bit application. This feature can be enabled by setting Index-20H bit 3 to 1. It will increase the write buffer burst capability to PCI bus. But for our testing, not every PCI VGA card can accept this feature currently. So, we suggest this feature programmed as an option in CMOS setup.

(e) CPU to PCI Write Buffer Burst:

This feature is used to enable PCI burst cycle defined in PCI specification. It is a very important feature for PCI performance. This feature can be enabled by setting Index-20H bit 4 to 1. This feature can always be enabled when CPU to PCI Write Buffer is enabled.

(f) CPU to PCI Write Buffer Fast-Back-to-Back:

This feature is used to enable PCI fast-back-to-back cycle defined in PCI specification. This feature can be enabled by setting Index-20H bit 5 to 1. But for our testing, not every PCI VGA card can accept this feature currently. So, we suggest this feature programmed as an option in CMOS setup.

(g) CPU to PCI Read/Write Cycle Address Issue 1 or 2 Cycles

This feature is used to solve the problem about the address hold time for some PCI cards especially implement BIOS on it. Those cards will design a latch signal to latch the ROM address by using TTL. Those cards need a critical address hold time for latch. This feature can be enabled by setting Index-21H bit 3 to 1. When this feature is enabled, M1489 will issue two cycles for address phase, that means FRAMEJ will assert two cycles and then issue IRDYJ.

6. M1489 PCI to CPU buffer programming

(a) PCI to CPU Read Buffer

This feature is used to enhance the PCI master read local memory performance. This feature can be enabled by setting Index-22H bit 0 to 1. M1489 implements a DWord read buffer.

(b) PCI to CPU Write Buffer

This feature is used to enhance the PCI master write local memory performance. This feature can be enabled by setting Index-22H bit 4 to 1. M1489 implements 2-lines write buffer. PCI master write local memory cycle will post to write buffer first to achieve 0 wait write cycle. After a line in write buffer is full, this line will burst write to local memory through the Burst Write Configuration(Index-22H bit 3). When 2 lines are full, M1489 can also be programmed to retry the PCI master or to wait until a line is flushed to local memory through the Retry/Wait Configuration (Index-22H bit 5).

7. M1487 System Arbitration

The M1487/M1489 arbitrated block supports 3 types of masters: the CPU processor, PCI masters and the DMA/ISA masters. A bus master is also the master of the entire system. M1487 arbiter supports 2 mode for selection. Arbiter mode 0 is using the sequence ISA->CPU->PCI0->PCI1->PCI2->CPU->ISA->CPU->PCI0->.... if all masters' request is asserted. This mode is suitable for applications when 3 PCI masters are used in motherboard. This mode treats each PCI master fair compare to DMA/ISA master. This mode is selected by resetting Index-28H bit 5 to 0. Each PCI master will occupy system bus for a time slot defined by Index-28H bits 3-0. Arbiter mode 1 is using the sequence ISA->CPU->PCI0->CPU->ISA->CPU->PCI1->CPU->ISA->CPU->PCI2->CPU->ISA->CPU->PCI0->CPU->.... if all masters' request is asserted. This mode is suitable for applications when ISA master or CPU needs more time to do the job. This mode is selected by setting Index-28H bit 5 to 1. PCI master broke function is defined by PCI specification. It is defined if arbiter granted PCI bus to a PCI master and that master did not issue FRAMEJ over 16 PCICLKs that means this PCI master is not normal. But for our testing, not every PCI master follows this specification to implement. So, if user wants to use this function, it had better use it as an option in CMOS setup.

8. PCI Interrupt Routine Table and Sensitive Control:

The M1487 supports 2 registers - Index 42h and 43h to define the routine mapping between PCI INT1~INT4 to ISA IRQ channels. The routine mapping table is described as below :

PCI INTx to ISA IRQ routine mapping table :

D3 D2 D1 D0 (D7 D6 D5 D4)	ISA mapping IRQ
0 0 0 0	Disable
0 0 1 0	IRQ3
0 1 0 0	IRQ4
0 1 1 0	IRQ7
1 0 0 0	reserved
1 0 1 0	reserved
1 1 0 0	reserved
1 1 1 0	reserved
0 0 0 1	IRQ9
0 0 1 1	IRQ10
0 1 0 1	IRQ5
0 1 1 1	IRQ6
1 0 0 1	IRQ11
1 0 1 1	IRQ12
1 1 0 1	IRQ14
1 1 1 1	IRQ15

And, the BIOS programmers should be inhibited to set PCI INTx to the reserved ISA IRQ channels. The PCI INTx sensitivity definition are defined in the Index-44h D3~D0. The PCI INTx level triggered signal will be transferred to ISA edge triggered when its respective bit be set to 1. Otherwise, the PCI INTX level triggered signal will be passed to ISA level triggered(programmed in port 4D0h and 4D1h) when its respective bit be set to 0.
Index-44h D0 : INT1 sensitivity setting for ISA
Index-44h D1 : INT2 sensitivity setting for ISA
Index-44h D2 : INT3 sensitivity setting for ISA

Index-44h D3 : INT4 sensitivity setting for ISA. Since these 4 bits are used to define the PCI INTx mapped ISA IRQs level/edge triggered sensitivity. The BIOS programmer should to keep the consistency of the mapped ISA sensitivity with the definition of the Port 4D0h and 4D1h.

The M1487 provides two 8 bit R/W registers for supporting ISA edge or level sensitive interrupts on a channel by channel basis. The two registers' are 04D0h for master interrupt controller and 04D1h for slave interrupt controller. These registers are used to set the interrupts to be triggered by either the signal edge or the logic level. IRQ0, IRQ1, IRQ2, IRQ8, IRQ13 must be set to edge sensitive for AT traditional usage. After the system reset all IRQ signals are set to edge sensitive. The description below shows which bit numbers represent the various IRQ signal.

(0 = edge sensitive; 1 = level sensitive.)

Port 04D0h	(R/W) 00h
D0	IRQ0 (should be kept at "0")
D1	IRQ1 (should be kept at "0")
D2	IRQ2 (should be kept at "0")
D3	IRQ3
D4	IRQ4
D5	IRQ5
D6	IRQ6
D7	IRQ7

Port 04D1h	(R/W) 00h
D0	IRQ8 (should be kept at "0")
D1	IRQ9
D2	IRQ10
D3	IRQ11
D4	IRQ12
D5	IRQ13 (should be kept at "0")
D6	IRQ14
D7	IRQ15

III. ISA System Bus/ System Controller Programming Reference Manual

9. TURBO Control:

(a) Hardware control:
When Index-2Bh D2 be set to "1", the status of TURBO switch will feed into M1487/M1489 via TURBO pin(pin 64 of M1487). And, this status can be read from Index-2Bh D3.

(b) Software control:
The software turbo control bit is in Index-2Bh D1. logic "1" means a turbo trigger event. A logic "0" means a deturbo trigger event.

(c) TURBO priority and status control :
When Index-2Bh D0 be set to "0"(HW TURBO HIGH first):

(1) If TURBO switch be set to "1"("TURBO"), the value of Index-2Bh D1 can NOT change the "TURBO" status.

(2) If TURBO switch be set to "0"("DETURBO"), the value of Index-2Bh D1 can change the "DETURBO" status. When Index-2Bh D0 be set to "1" (HW/SW equal priority), the current event trigger (no matter by HW or SW) will override the previous status.

(d) The system turbo status can be read from Index-2Bh D4.

(e) DETURBO methods of M1487/M1489:

The DETURBO recommended algorithm of M1487/M1489 is to down-grade the CPU performance by issuing a CLKCTR(pin 72 of M1487) logic "0" to control the external clock generator(level-control). But, the hardware Turbo pin transition events also can be optionally used to produce a latch triggered control via CLKCTR and MAs signals(latch-control) or a SMI request to CPU(SMI control via the software effort) by programming the Index-40h D0~D4.

IV. M1489/M1487 PMU Software Programming Reference Manual

10. Power Management Control

(a) PMU(power management unit) feature control:
PMU feature control bit is in Index-30h D2.
When Index-30h D2 = "1" , PMU feature will be enabled.
When Index-30h D2 = "0" , PMU feature will be disabled. (When PMU feature be disabled, the D7~D4 of Index-35h should be written back to their default value "0h".)

(b) PMU mode definition are in Index-30h D1~D0.

11. M1489/M1487 SMI routine initialization procedure:

(a) Unlock sequence:

(1) output port 22h, data 03h

(2) output port 23h, data C5h
then, the M1487/M1489 configuration registers are all accessible.

(b) Initialization sequence:

(1) Set CPU type for Intel/AMD/Cyrix SMI/SMM mode:
Programming the Index-35h D7~D6.
Programming the Index-35h D5~D4 for SMI trigger feature.

(2) Set Index-19h D3 to logic '1'--> enable SMM be accessible in normal cycle

(3) Load SMI routine to SMM region(i.e. 38000h for Intel, 68000h for AMD) --> move the SMI routine to 38000h (68000h)
(4) Set Index-19h D3 to logic '0'

--> disable SMM be accessible in normal cycle. The following steps is used for SMM region relocation scheme :

(5) Enable the software SMI function :
Programming the Index-30h D2 -> "1", Index-30h D4 -> "1", programming the Index-30h D3 -> "1" for software SMI. (Wait for softSMI)

(6) SMI routine
Read SMI cause by Index-35h D3~D0 reading :
Index35h D3~D0 = "Eh" (softSMI)
Set the Index-30h D4 -> "0" (clear SMI event)
Set the Index-30h D3 -> "0" (clear softSMI trigger)
Programming the CPU internal registers SMM mapping address to relocated region(A/B/E). Set the Index-30h D4 -> "1" (enable SMI event : optional)
Set the Index-3Dh D2 -> "1" (chip RSM) RSM instruction

(7) After SMI routine is executed:
Programming the Index-19h D5~D4 for SMM mapping relocated definition which should be consistent with the CPU registers setting.

Note:

1. When Index-19h D3 is set to "1", the SMM region memory is visible at normal cycle(not in SMI routine). i.e. the SMM can be accessible when CPU issues a SMMBASE segment memory cycle in the normal operation. This action should be done before O.S. or program is loaded because of the in-visible original normal memory of SMMBASE segment. So, this function can initialize the SMM memory code for the later SMI use. When Index-19h D3 is set to "0", the SMM region memory is visible only at SMI cycle(routine). This bit should be set to "0" after the SMM memory initialization.

2. The Index-19h D5~D4 for SMM mapping reallocation should be programmed according to CPU internal SMMBASE definition.

3. If CPU SMMBASE and M1489/M1487 Index-19h D5~D4 are programmed as E segment(E0000h ~ EFFFFh), there are two ways to access E region memory. The access of E segment in normal CPU cycle is treated according to shadow region R/W definition(Index- 14h D1~D0, D5~D4). But when Index-19h D3='1' or CPU is in SMI status , the E segment is accessed as SMM region which is Read/Write enabled.

4. If CPU SMMBASE and M1489/M1487 Index-19h D5~D4 are programmed as AB segment(A0000h ~ BFFFFh), the access of AB region when Index-19h D3='1'(refer to Note 1.) or CPU is in SMI status is directed to SMM RAM, but not ISA (or PCI) slot memory. Under this condition, the access of VGA AB region memory is achieved by setting Index-19h D0 to '1'. In other words, when SMM RAM is reallocated to AB segment and Index-19h D0='0', the access to AB region is treated as SMM RAM access. On the other hand, when SMM RAM is reallocated to AB segment and Index-19h D0='0', the access to AB region is still ISA/PCI slot memory access.

(c) SMI/SMM control and SMM region mapping control:

The SMI and SMM default control bits are defined in Index-35h D7~D6. The following table describes the default SMM mapping region:

D7 D6	CPU Type	SMM region
0 0	Intel compatible	30000 ~ 3FFFF
0 1	Cyrix compatible	30000 ~ 3FFFF
1 0	AMD compatible	60000 ~ 6FFFF
1 1	reserved	reserved

12. M1489/M1487 SMI event control:

SMI event can be implemented by four methods:
(1) SMI signal pin (green CPU)
(2) NMI signal pin (non-green CPU)
(3) IRQ15 signal pin (non-green CPU)
(4) IRQ10 signal pin (non-green CPU)

These setting can be programmed in Index-35h D5~D4. SMI can be generated by 13 events which are defined in Index-33h D7~D0, Index-34h D4~D0. The SMI events' cause can be read from Index-35h D3~D0. The procedure of SMI control is as below:
(1) enter SMI routine:
Read Port 22h for storing the port-22h data.
Store the port-70h data by reading the Index-3Fh (shadow Port 70h) data.
(2) read SMI events' cause for Index-35h.
(3) clear SMI signal by setting Index-30h D4 to "0".
(4) clear SMI source event(such as timer, ...).
(5) SMI main service routine.
(6) enable SMI signal by setting Index-30h D4 to "1".
(7) Leave SMI routine :
Restore the port-70h data Chip RSM setting by programming Index-3Dh D2 to "1".
Restore the port-22h data
RSM instruction

Please refer to the SMI control flowchart.
The software SMI can be asserted by setting the Index-30h D3 to "1".

13. PMU timers setting:

The M1489/M1487 supports 3 timers for monitoring the system mode, GP/MEM, and Input_device activity.

(a) system mode timer setting:

The monitored event of the system mode can be selected by programming the Index-31h, Index-32h D2~D0. The VGA monitored range are defined in Index-3Ch D1~D0. The GP/IO monitored range are defined in Index-3Ch D4~D2. The GP/MEM range can be defined by programming the Index-25h ~Index-27h. The address mask bits of GP/MEM be set to "1" mean that their respective address bits will be ignored in the range checking. The monitored event (IRQ3, IRQ4, and IRQ12) of Input_device are defined in Index-32h D7~D5. The setting of IRQ group be defined in the Index-36h and 37h. The setting of DRQ group be defined in the Index-38h. The setting of the system mode timer is defined in Index-39h. The D0~D1 of this Index are the time base (unit) setting. The D2 is the timer count or reset (clear) control bit. The D7~D4 are the timer time-out period setting. And, when Index-3Dh D1 = "0", the D7~D4 will be read as the timer time-out setting; When Index-3Dh D1 = "1", the D7~D4 will be read as the timer counter current value.

When Index-34h D7 be set to "1", the time base(unit) of all timers will be double. When this timer timeout SMI be issued, this triggering timer should be clear/ reset after reading the cause of SMI event in SMI routine.

The following steps are the mode timer programming example :

(1) Enable the PMU function:
Programming the Index-30h D2 to "1".
Programming the Index-30h D1D0 to the proper system state.

(2) Set the monitored condition:
Programming the Index-3Ch D1D0 for VGA. Programming the Index-3Ch D4D2 for GP/IO. Programming the Index-25h ~ 27h for GP/MEM. Programming the Index-32h D7~D5 for Input_device. Programming the Index-36h, 37h for IRQ group.
Programming the Index-38h for DRQ group.

(3) Set the monitored events:
Programming the Index-31h, 32h D2~D0 for mode timer monitored events selection.

(4) Set the SMI triggered by mode timer timeout:
Programming the Index-33h D0 to "1".

(5) Set the mode timer:
Programming the Index-39h D1D0 for time-base setting.
Programming the Index-39h D7~D4 for time-out count setting.
Programming the Index-39h D2 to "1" for timer count start.

(6) Enable SMI function :
Programming the Index-30h D4 to "1".
..... (Wait for Mode timer timeout SMI)

(7) SMI routine
Enter SMI routine:
Read Port 22h for storing the port-22h data.
Store the port-70h data by reading the Index-3Fh(shadow Port 70h) data.
Read SMI cause by Index-35h D3~D0 reading:
Index35h D3~D0 = "1h" (Mode timeout SMI)
Set the Index-30h D4 -> "0" (clear SMI event)
Set the Index-39h D2 -> "0" (clear timer)
*** Mode timer timeout main program.
Set the next system mode state by programming Index-30h D1D0.
load the next state monitored events by programming Index- 31h, 32h D2~D0.
load the next state timer setting by programming Index-39h.
Set the Index-30h D4 -> "1" (enable SMI event)
Leave SMI routine:
Restore the port-70h data Chip RSM setting by programming Index-3Dh D2 to "1".
Restore the port-22h data RSM instruction

(b) Input_device timer setting:

The monitored event of the Input_device can be selected by programming the Index-32h D7~D5.
The setting of the Input_device timer is defined in Index-3Ah.
The following steps are the Input_device timer programming example:

(1) Enable the PMU function:
Programming the Index-30h D2 to "1".

(2) Set the monitored condition:
Programming the Index-32h D7~D5 for Input_device.

(3) Set the SMI triggered by Input_device timer timeout:
Programming the Index-33h D1 to "1".

(4) Set the mode timer:
Programming the Index-3Ah D1D0 for time-base setting.
Programming the Index-3Ah D7~D4 for time-out count setting.
Programming the Index-3Ah D2 to "1" for timer count start.

(5) Enable SMI function:
Programming the Index-30h D4 to "1".
(Wait for Input_device timer timeout SMI)

(6) SMI routine
Enter SMI routine:
Read Port 22h for storing the port-22h data.
Store the port-70h data by reading the Index-3Fh(shadow Port 70h) data. Read SMI cause by Index-35h D3~D0 reading:
Index35h D3~D0 = "2h" (Input_device timeout SMI)
Set the Index-30h D4 -> "0" (clear SMI event)
Set the Index-3Ah D2 -> "0" (clear timer)
*** Input_device timer timeout main program.
Set the Index-30h D4 -> "1" (enable SMI event, optional)
Leave SMI routine:
Restore the port-70h data Chip RSM setting by programming Index-3Dh D2 to "1". Restore the port-22h data RSM instruction

(c) GP/MEM timer setting:
The monitored region of the GP/MEM can be defined by programming the Index-25h to Index-27h. The setting of the GP/MEM timer is defined in Index-3Bh.

The following steps are the GP/MEM timer programming example :

(1) Enable the PMU function:
Programming the Index-30h D2 to "1".

(2) Set the monitored region:
Programming the Index-25h to Index-27h for GP/MEM.

(3) Set the SMI triggered by GP/MEM timer timeout:
Programming the Index-33h D2 to "1".

(4) Set the mode timer:
Programming the Index-3Bh D1D0 for time-base setting.
Programming the Index-3Bh D7~D4 for time-out count setting.
Programming the Index-3Bh D2 to "1" for timer count start.

(5) Enable SMI function:
Programming the Index-30h D4 to "1".
(Wait for Input_device timer timeout SMI)

(6) SMI routine
Enter SMI routine:
Read Port 22h for storing the port-22h data. Store the port-70h data by reading the Index-3Fh(shadow Port 70h) data.
Read SMI cause by Index-35h D3~D0 reading :
Index35h D3~D0 = "3h" (GP/MEM timeout SMI)
Set the Index-30h D4 -> "0" (clear SMI event)
Set the Index-3Bh D2 -> "0" (clear timer)
*** GP/MEM timer timeout main program.
Set the Index-30h D4 -> "1" (enable SMI event, optional)
Leave SMI routine:
Restore the port-70h data Chip RSM setting by programming Index-3Dh D2 to "1". Restore the port-22h data RSM instruction

14. IRQ/DRQ group event definition:

The IRQs group event is defined in Index-36h and Index-37h. The IRQs event (excluding Input_device IRQ events) will be qualified with the M8259, interrupt controllers, IMR (mask registers) setting. The DRQs group event (including the PCI master request events) is defined in Index-38h. The DRQs event will be optionally qualified with the M8237, DMA controllers, DMR setting by programming the Index-32h D3.

15. Trigger SMI setting:

The M1489/M1487 supports 5 types of trigger SMI function: IRQs active, DRQs active, Input_device active access, RTC alarm, and EXTSW event.

(a) IRQs active SMI setting:
The following steps are the IRQs active SMI programming example:

(1) Enable the PMU function:
Programming the Index-30h D2 to "1".

(2) Set the IRQ monitored events:
Programming the Index-36h to Index-37h for IRQ group.

(3) Set the SMI triggered by IRQ active:
Programming the Index-33h D5 to "1".

(4) Enable SMI function:
Programming the Index-30h D4 to "1".
(Wait for IRQ active SMI)

(5) SMI routine
Enter SMI routine:
Read Port 22h for storing the port-22h data.
Store the port-70h data by reading the Index-3Fh(shadow Port 70h) data.
Read SMI cause by Index-35h D3~D0 reading:
Index35h D3~D0 = "6h" (IRQ active SMI)
Set the Index-30h D4 -> "0" (clear SMI event)
Set the Index-33h D5 -> "0" (clear IRQ active event)
*** IRQ active SMI main program.
Set the Index-30h D4 -> "1" (enable SMI event, optional)
Set the Index-33h D5 -> "1" (enable IRQ active event, optional)
Leave SMI routine:
Restore the port-70h data Chip RSM setting by programming Index-3Dh D2 to "1". Restore the port-22h data

(b) DRQs active SMI setting:
The following steps are the DRQs active SMI programming example:

(1) Enable the PMU function:
Programming the Index-30h D2 to "1".

(2) Set the IRQ monitored events:
Programming the Index-38h for DRQ group.

(3) Set the SMI triggered by DRQ active :
Programming the Index-33h D6 to "1".

(4) Enable SMI function:
Programming the Index-30h D4 to "1".
(Wait for DRQ active SMI)

(5) SMI routine
Enter SMI routine:
Read Port 22h for storing the port-22h data.
Store the port-70h data by reading the Index-3Fh (shadow Port 70h) data.
Read SMI cause by Index-35h D3~D0 reading:
Index35h D3~D0 = "7h" (DRQ active SMI)
Set the Index-30h D4 -> "0" (clear SMI event)
Set the Index-33h D6 -> "0" (clear DRQ active event)
*** DRQ active SMI main program.
Set the Index-30h D4 -> "1" (enable SMI event, optional)
Set the Index-33h D6 -> "1" (enable DRQ active event, optional)
Leave SMI routine:
Restore the port-70h data Chip RSM setting by programming Index-3Dh D2 to "1". Restore the port-22h data

(c) Input_device active SMI setting:
The following steps are the Input_device active SMI programming example:

(1) Enable the PMU function:
Programming the Index-30h D2 to "1".

(2) Set the Input_device monitored events:
Programming the Index-32h D7~D5 for Input_device selection.

(3) Set the SMI triggered by Input_device active:
Programming the Index-33h D4 to "1".

(4) Enable SMI function:
Programming the Index-30h D4 to "1".
(Wait for Input_device active SMI)

(5) SMI routine
Enter SMI routine:
Read Port 22h for storing the port-22h data.
Store the port-70h data by reading the Index-3Fh(shadow Port 70h) data. Read SMI cause by Index-35h D3~D0 reading:
Index35h D3~D0 = "5h" (Input_device active SMI)
Set the Index-30h D4 -> "0" (clear SMI event)
Set the Index-33h D4 -> "0" (clear Input_device active event)
*** Input_device active SMI main program.
Set the Index-30h D4 -> "1" (enable SMI event, optional)
Set the Index-33h D4 -> "1" (enable Input_device active event, optional)
Leave SMI routine:
Restore the port-70h data
Chip RSM setting by programming Index-3Dh D2 to "1".
Restore the port-22h data

(d) RTC alarm active SMI setting:
The following steps are the RTC alarm active SMI programming example:

(1) Enable the PMU function :
Programming the Index-30h D2 to "1".

(2) Programming the RTC alarm time.

(3) Set the SMI triggered by RTC alarm active:
Programming the Index-33h D3 to "1".

(4) Enable SMI function:
Programming the Index-30h D4 to "1".
(Wait for RTC alarm active SMI)

(5) SMI routine
Enter SMI routine:
Read Port 22h for storing the port-22h data.
Store the port-70h data by reading the Index-3Fh(shadow Port 70h) data. Read SMI cause by Index-35h D3~D0 reading:
Index35h D3~D0 = "4h" (RTC alarm active SMI)
Set the Index-30h D4 -> "0" (clear SMI event) Set the Index-33h D3 -> "0" (clear RTC alarm active event)
*** RTC alarm active SMI main program.
Set the Index-30h D4 -> "1" (enable SMI event, optional)
Set the Index-33h D3 -> "1" (enable RTC alarm active event, optional)
Leave SMI routine:
Restore the port-70h data
Chip RSM setting by programming Index-3Dh D2 to "1".
Restore the port-22h data

(e) EXTSW(suspend button) active SMI setting:
The following steps are the EXTSW active SMI programming example:

(1) Enable the PMU function:
Programming the Index-30h D2 to "1".

(2) Programming the EXTSW active polarity in the Index-34h D6D5.

(3) Set the SMI triggered by EXTSW active:
Programming the Index-33h D7 to "1".
(4) Enable SMI function:
Programming the Index-30h D4 to "1".
(Wait for EXTSW active SMI)

(5) SMI routine
Enter SMI routine :
Read Port 22h for storing the port-22h data.
Store the port-70h data by reading the Index-3Fh (shadow Port 70h) data.
Read SMI cause by Index-35h D3~D0 reading:
Index35h D3~D0 = "8h" (EXTSW active SMI)
Set the Index-30h D4 -> "0" (clear SMI event)
Set the Index-33h D7 -> "0" (clear EXTSW active event)
*** EXTSW active SMI main program.
Set the Index-30h D4 -> "1" (enable SMI event, optional).
Set the Index-33h D7 -> "1" (enable EXTSW active event, optional). Leave SMI routine:
Restore the port-70h data Chip RSM setting by programming Index-3Dh D2 to "1". Restore the port-22h data

16. Access SMI setting for I/O trap feature:

The M1489/M1487 supports 5 monitored access events for I/O trap function:
VGA access, HDD access, LPT access, GP/IO access, and GP/MEM access event.

The following steps are the I/O trap (Access) SMI programming example:
(1) Enable the PMU function :
Programming the Index-30h D2 to "1".

(2) Set the related device to power-saving mode.

(3) Set the monitored condition:
Programming the Index-3Ch D1D0 for VGA.
Programming the Index-3Ch D4D2 for GP/IO.
Programming the Index-25h ~ 27h for GP/MEM.

(4) Set the SMI triggered by trap access events:
Programming the Index-34h D4~D0 related bit to "1".

(4) Enable SMI function:
Programming the Index-30h D4 to "1".
(Wait for I/O trap SMI)

(5) SMI routine
Enter SMI routine:
Read Port 22h for storing the port-22h data.
Store the port-70h data by reading the Index-3Fh (shadow Port 70h) data.
Read SMI cause by Index-35h D3~D0 reading:
Index35h D3~D0 = "9h"-"Dh" (Trap SMI)
Set the Index-30h D4 -> "0" (clear SMI event)
Set the Index-34h related bit -> "0" (clear trap event)
*** I/O Trap SMI main program.
Set the Index-30h D4 -> "1" (enable SMI event, optional)
Leave SMI routine:
Restore the port-70h data Chip RSM setting by programming Index-3Dh D2 to "1". Restore the port-22h data

17. STOP-CLOCK control:

(a) Software STOP-CLOCK activated control :
When Index-30h D5 be set to "1", the M1489/ M1487 will issue a software STOP-CLOCK activated event. This bit will automatically reset to "0" when the STOP-CLOCK be de-activated.

(b) STOP-CLOCK de-activated control:
The STOP-CLOCK can be de-activated by SMI, IRQ/NMI, or DRQ/ ISA/ PCI-Master request events. The SMI event will always deactivate the STOP-CLOCK signal. But the IRQ/NMI or DRQ/ISA/PCI-Master request can be programmed to deactivated the STOP-CLOCK or not.
INTR/NMI events:
When Index-30h D7="1", the IRQ/NMI events will NOT deactivate the STOP-CLOCK. When Index-32h D7="0", the IRQ/NMI can be individually selected by programming Index-36h and 37h to deactivate the STOP-CLOCK.
DRQ/ISA/PCI-Master events:
When Index-30h D6="1", the DRQ/ISA/PCI-master events will NOT deactivate the STOP-CLOCK. When Index-30h D6="0", the DRQ/ISA/PCI-master events will deactivate the STOP-CLOCK.

(c) CLOCK Throttling Feature:
The CLOCK throttling feature can be programmed in Index-32h D4. The M1487/M1489 hardware will automatically activate the STOP-CLOCK signal when the internal idle timer timeout. And, the de-activated events be controlled as the above de-activated control description.

18. Power-control signals:

(a) Power-control using by latched element:
(the CLKCTR pin of M1487 is used to latch the power-control signals). The 8 power-control signals are defined in Index-41h (PWR7~PWR0), the hardware control setting can be read from these registers before programming them. The procedure of output the newer control data are:
(1) write the Index-40h D2 to "1".
(2) write the control data to Index-41h PWR7~ PWR0 (mapped to MA7~0).
(3) write the Index-40h D0 to "0".

(b) Power-control using by level setting element:
(the CLKCTR pin of M1487 is used to indicate the power-control status). The procedure of output the newer control data are:
(1) write the Index-40h D2 to "0".
(2) write the Index-40h D0 to "0" for power-saving control, or write the Index-40h D0 to "1" for full-on operation control.

19. MODE LED control:

The MODE LED for indicating the system mode state can be programmed in Index-3Ch D7~D5.

20. PMU NOTE:
(1) The SMI control procedure can be referred to from the SMI control flowchart (Section 6, Fig. 3, p.126).
(2) The STOP-CLOCK control procedure can be referred to from the STPCLKJ signal control flowchart (Section 6, p.127).
(3) The Power-control procedure can be referred to from the Power output signals programming flowchart (Section 6, Fig 6, p 132).

Section 6: Design Issues

MA TABLE

TABLE 1 **32 BIT System MA Table 1**

	256K-COL	256K-ROW	1M-COL	1M-ROW	4M-COL	4M-ROW	512K-COL	512K- ROW	16M-COL	16M-ROW
MA0	A3	A14	A3	A14	A3	A14	A3	A14	A3	A14
MA1	A4	A15	A4	A15	A4	A15	A4	A15	A4	A15
MA2	A5	A16	A5	A16	A5	A16	A5	A16	A5	A16
MA3	A6	A17	A6	A17	A6	A17	A6	A17	A6	A17
MA4	A7	A18	A7	A18	A7	A18	A7	A18	A6	A18
MA5	A8	A19	A8	A19	A8	A19	A8	A19	A8	A19
MA6	A9	A11	A9	A20	A9	A20	A9	A20	A9	A20
MA7	A10	A12	A10	A21	A10	A21	A10	A12	A10	A21
MA8	A2	A13	A2	A13	A2	A22	A2	A13	A2	A22
MA9			A11	A12	A11	A23		A11	A11	A23
MA10					A12	A13			A12	A24
MA11									A13	A25

TABLE 2 **32 BIT System MA Table 1**

	2M-COL	2M-ROW	2M-COL	2M-ROW	4M-COL	4M-ROW	1M-COL	1M-ROW
MA0	A3	A14	A3	A14	A3	A14	A3	A14
MA1	A4	A15	A4	A15	A4	A15	A4	A15
MA2	A5	A16	A5	A16	A5	A16	A5	A16
MA3	A6	A17	A6	A17	A6	A17	A6	A17
MA4	A7	A18	A7	A18	A7	A18	A7	A18
MA5	A8	A19	A8	A19	A8	A19	A8	A19
MA6	A9	A20	A9	A20	A9	A20	A9	A20
MA7	A10	A21	A10	A21	A10	A21	A2	A21
MA8	A2	A22	A2	A22	A2	A22		A13
MA9	A11	A12		A12	A11	A23		A12
MA10		A13		A13		A13		A10
MA11				A11		A12		A11

CACHE MAPPING TABLE

1 BANK CACHE for 486 system (Line length = 16 bytes)

Cache Size	Tag Size	Memory Mapping (Data, Tag)		Cacheable Region
(32Kx8) x4	8Kx7	A4.....A16,	A17.....A23	16 MB
128K	8Kx8	A4.....A16,	A17.....A24	32 MB
(64Kx8) x4	16Kx7	A4.....A17,	A18.....A24	32 MB
256K	16Kx8	A4.....A17,	A18.....A25	64 MB
(128Kx8) x4	32Kx7	A4.....A18,	A19.....A25	64 MB
(512K	32Kx8	A4.....A18,	A19.....A26	128 MB
		Data SRAM	TAG SRAM	

2 BANK CACHE for 486 system (Line length = 16 bytes)

Cache Size	Tag Size	Memory Mapping (Data, Tag)		Cacheable Region
(32Kx8) x4	8Kx7	A4.....A16,	A17.....A23	16 MB
128K	8Kx8	A4.....A16,	A17.....A24	32 MB
(64Kx8) x4	16Kx7	A4.....A17,	A18.....A24	32 MB
256K	16Kx8	A4.....A17,	A18.....A25	64 MB
(128Kx8) x4	32Kx7	A4.....A18,	A19.....A25	64 MB
512K	32Kx8	A4.....A18,	A19.....A26	128 MB
		Data SRAM	TAG SRAM	

NOTE: TAG size x Kx7 means using L2 tag 7 bit with 1 'Dirty bit
TAG size x K x8 means using L2 tag 8 bit feature
The 1st |.....| is the DATA SRAM mapping address
The 2nd |.....| is the TAG SRAM mapping address

Cache Timing Quick Reference Table

	Read Hit		Cycle	
	2 bank	cache	1 bank	cache
Chk-pt	fast(0Wait)	normal(1Wait)	fast(0W)	normal(1W)
Fastest	2-1-1-1	3-2-2-2	2-1-1-1	3-2-2-2
Fast	3-1-1-1	4-2-2-2	3-1-1-1	4-2-2-2
Normal	4-1-1-1	5-2-2-2	4-1-1-1	5-2-2-2

	Write Hit		Cycle	
	2 bank	cache	1 bank	cache
Chk-pt	fast	normal	fast	normal
Fastest	2-1-1-1	3-2-2-2	2-2-2-2	3-3-3-3
Fast	3-1-1-1	4-2-2-2	3-2-2-2	4-3-3-3
Normal	4-1-1-1	5-2-2-2	4-2-2-2	5-3-3-3

0W: zero wait
1W: one wait

DRAM Timing Quick Reference Table

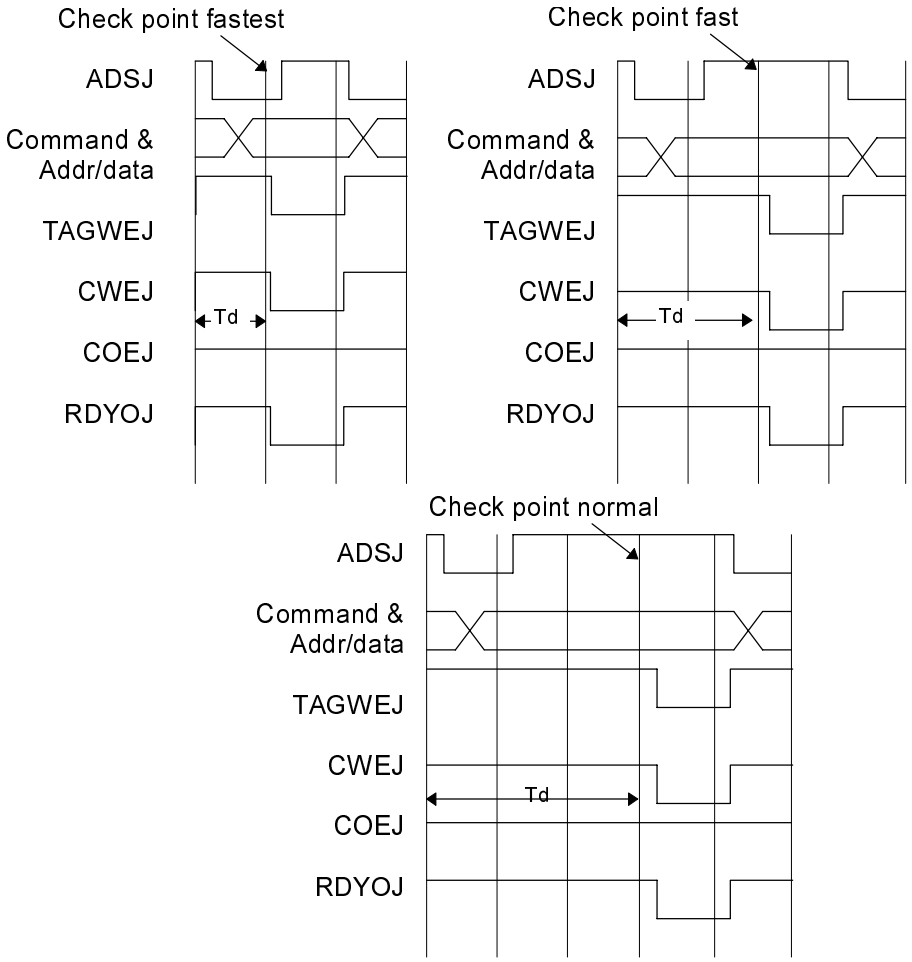
DRAM Set	**Fastest**	**Fast**	**Normal**	**Slow**	
Trp	2T	2T	3T	3T	RAS precharge time
Trcd	2T	2T	2T	3T	RAS-to-CAS delay
Tcas	1T	2T	3T	4T	read CAS pulse width
Twcp	1T	2T	3T	4T	Write CAS precharge time
Twp	1T	1T	1T	1T	Write CAS pulse width
Trcp	1T	1T	1T	1T	Read CAS precharge time

UNIT : CPUCLK

CHECK POINT

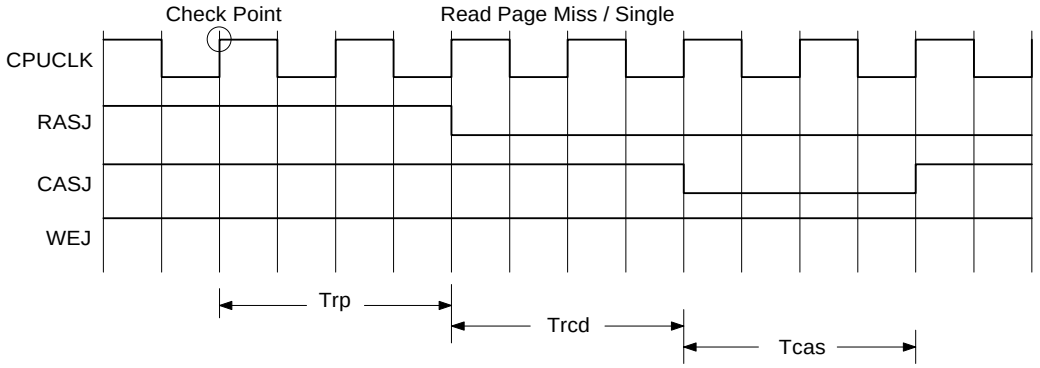
M1489/M1487 check DRAM/Cache read hit/miss or write hit/miss at check point.
The slower check point has more decoded time and the system will be more stable.
But the system performance will be slow.

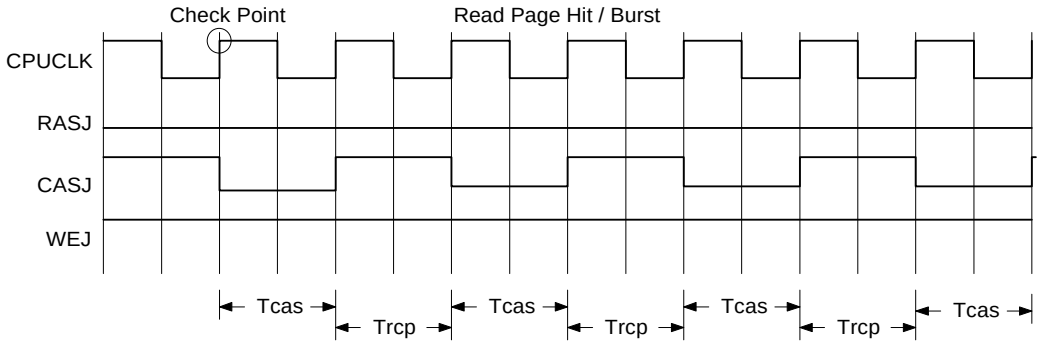
ex. Cache write hit



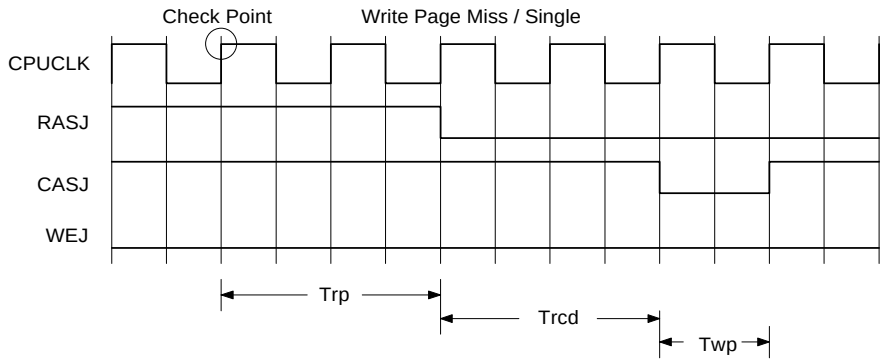
Td - Decode time

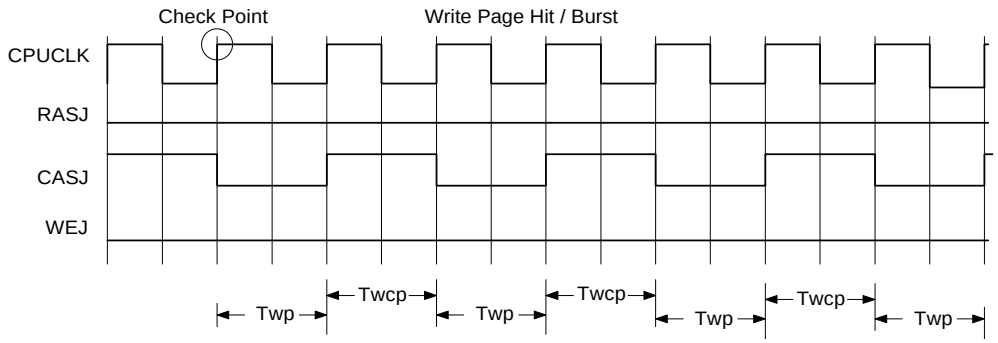
DRAM Read Access Timing





DRAM Write Access Timing





LINK-BUS PACKET DEFINITION

	15	14	13	12	11.....8	7	6	5.....0
C1	ROM	M/IO	D/C	W/R	BE[3-0]	Reserved		Address[23-18]
C2	Address [17-2]							
D1	Data [15-0]							
D2	Data [31-16]							
G/A	Go(1001)/Abort(1010)				Reserved			Green & Parity Status

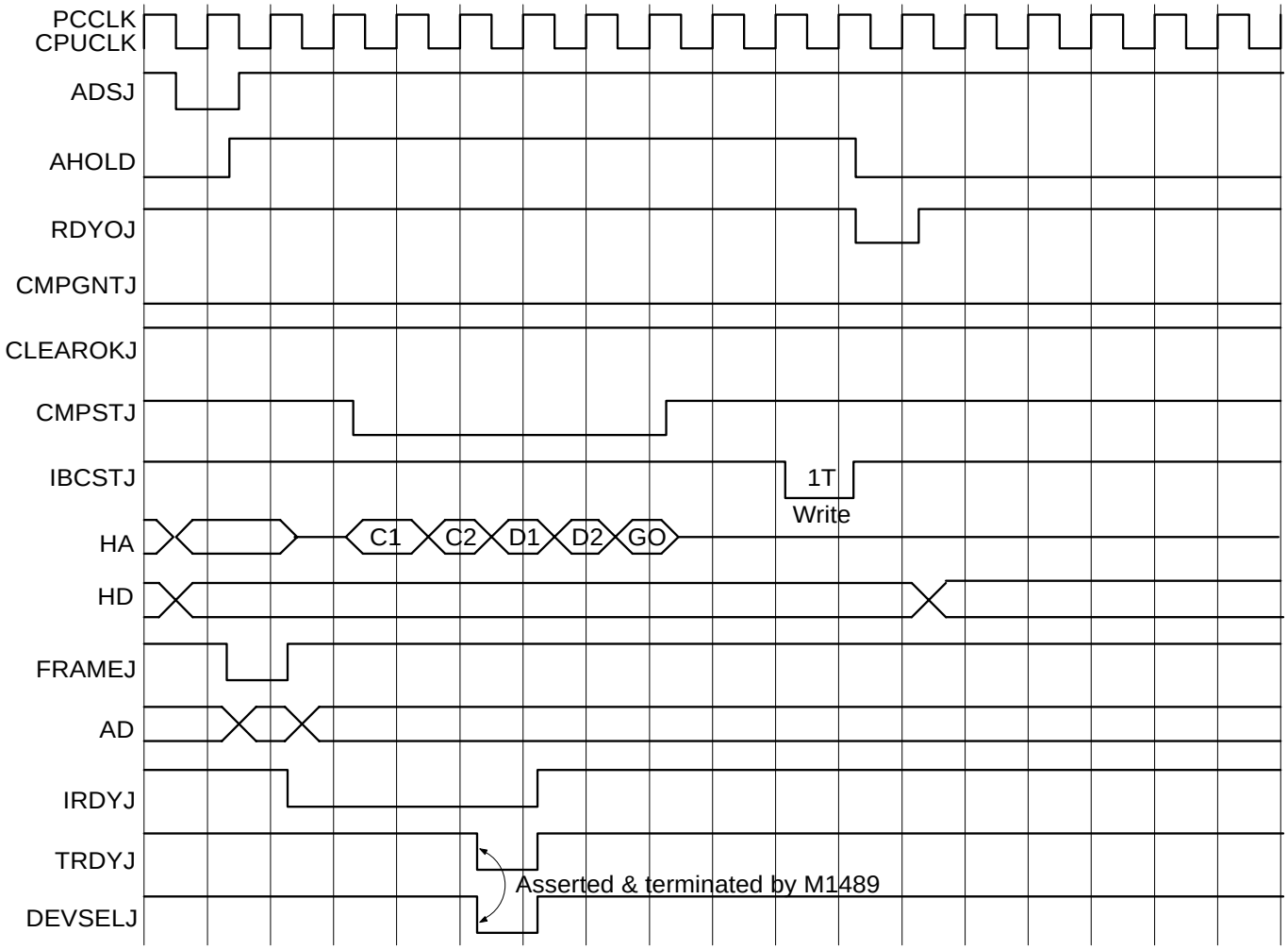
Packet Format Write

Go = 1001
Abort = 1010
ROM : A31,A26-A24 all '1'
Green & Parity Status bits are used to indicate the monitored events for PMU and the parity error status

	15	14	13	12	11.....8	7	6	5.....0
C1	ROM	M/IO	D/C	W/R	BE[3-0]	Reserved		Address[23-18]
C2	Address [17-2]							
G/A	Go/Abort				Reserved			Green & Parity Status
D1	Data [15-0]							
D2	Data [31-16]							

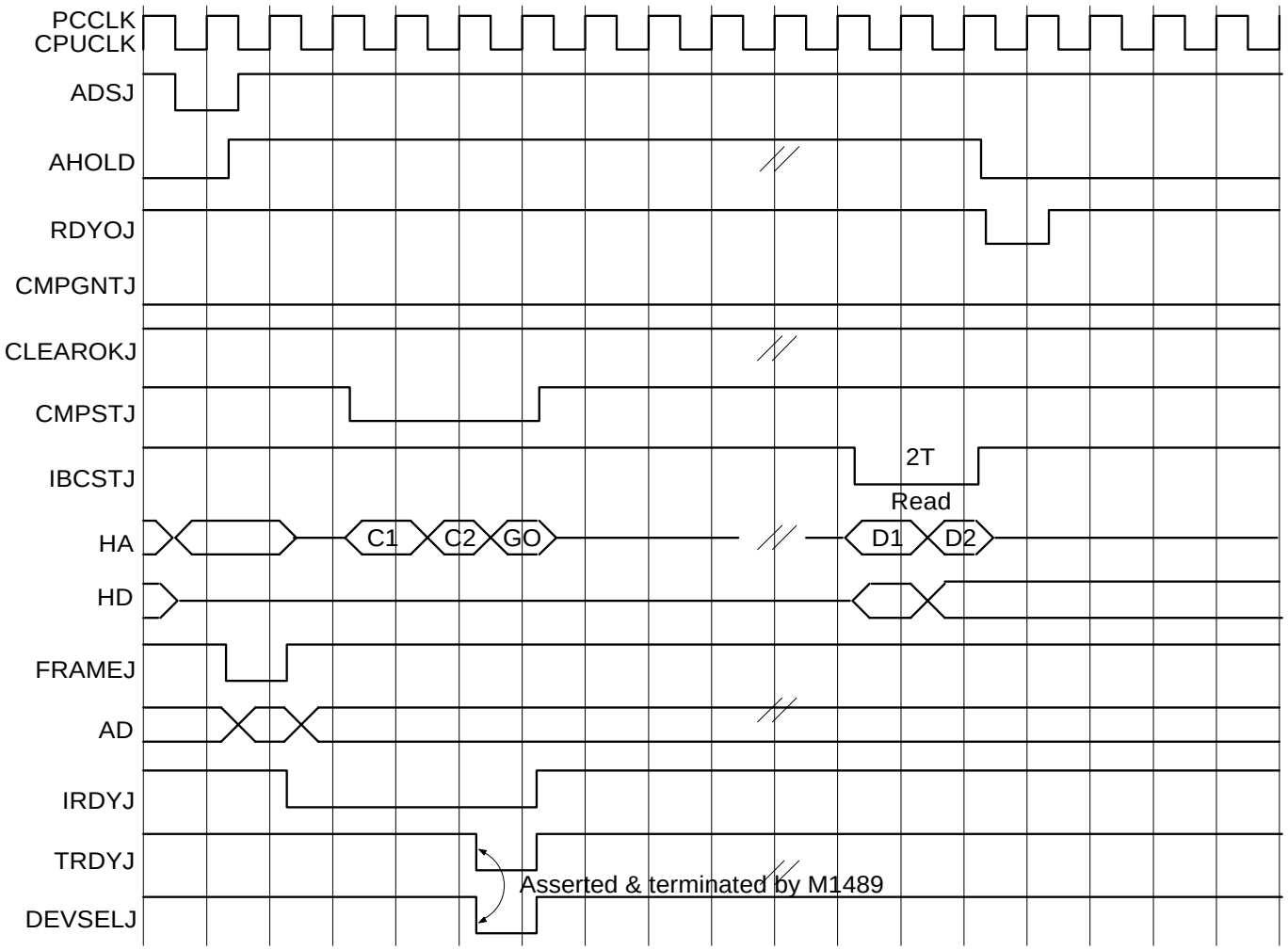
Packet Format Read

LINK-BUS TIMECHART1



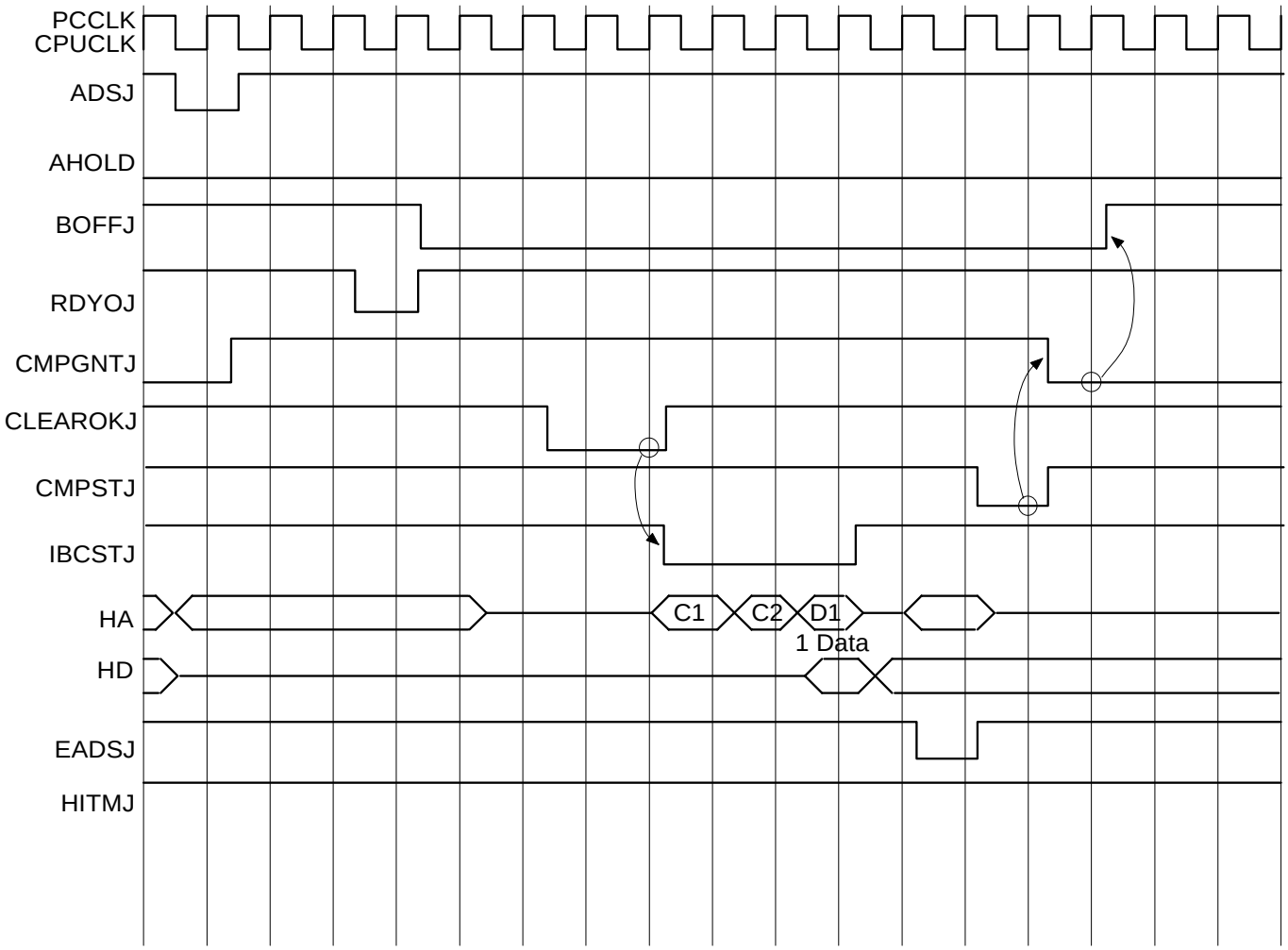
CPU write acess ISA slave

LINK-BUS TIMECHART2



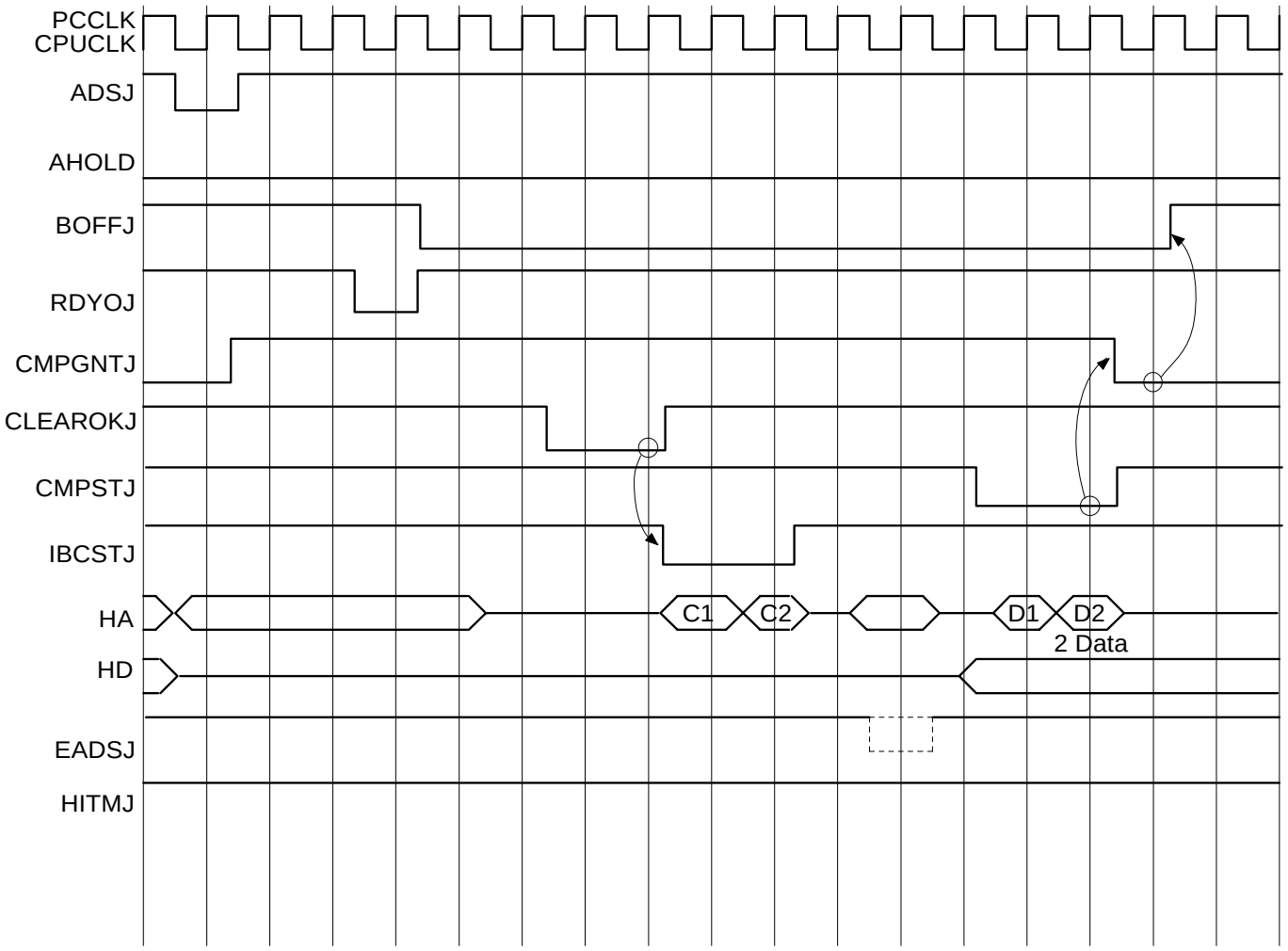
CPU read acess ISA slave

LINK-BUS TIMECHART3

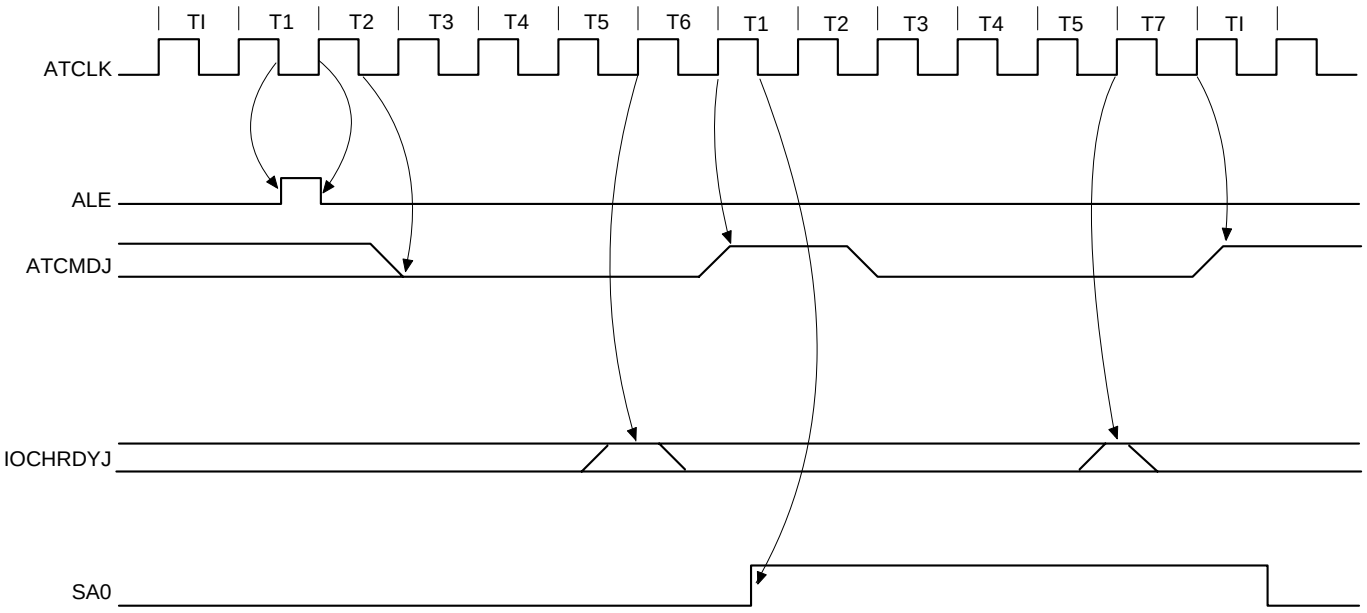


ISA Master/DMA write access local memory

LINK-BUS TIMECHART4



ISA Master/DMA read access local memory

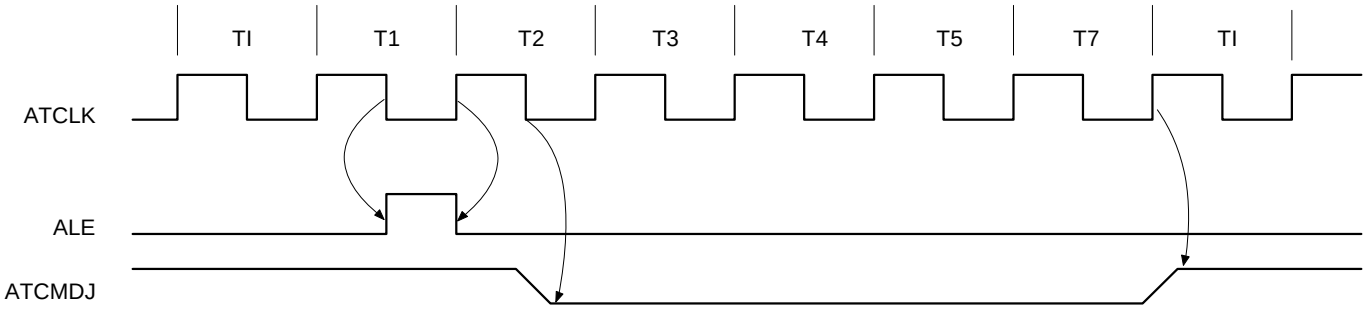


IOCHRDYJ INACTIVE
OWS INACTIVE
IF IOCHRDYJ IS INACTIVE, CYCLE WILL BE ADDED AT T5.
IF OWSJ IS ACTIVE AT T2,..T4, THE CYCLE WILL GO INTO T6.

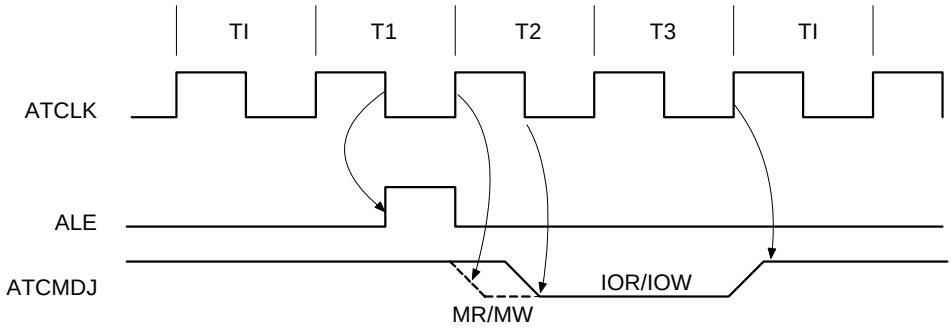
NOTE: IOCHRDYJ will be sampled in ATCLK falling

ISA Word_Byte Converting Timing

BYTE-OPERATION



WORD-OPERATION



ISA slave access timing

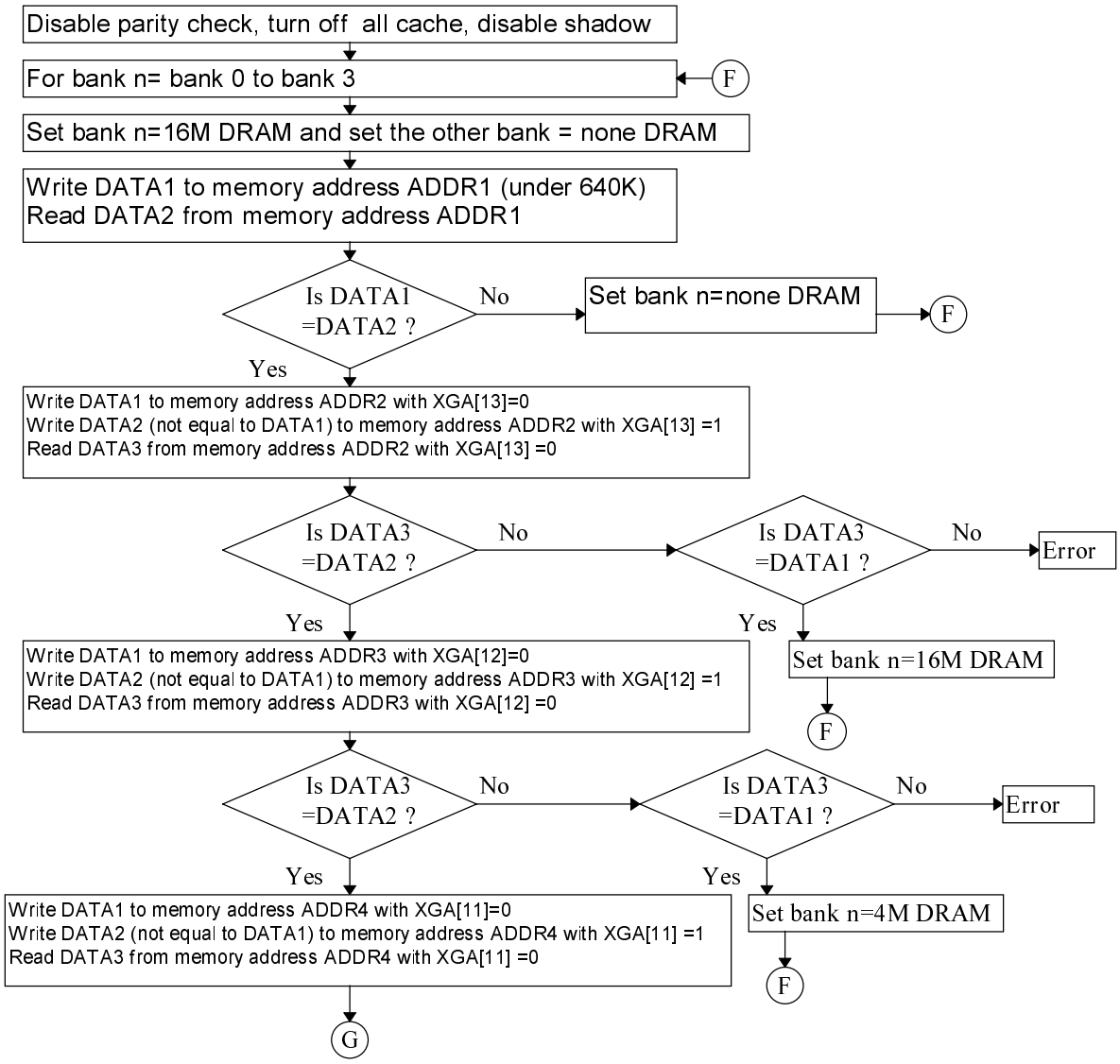


Figure 1-1. Memory Autosizing Flowchart - 1

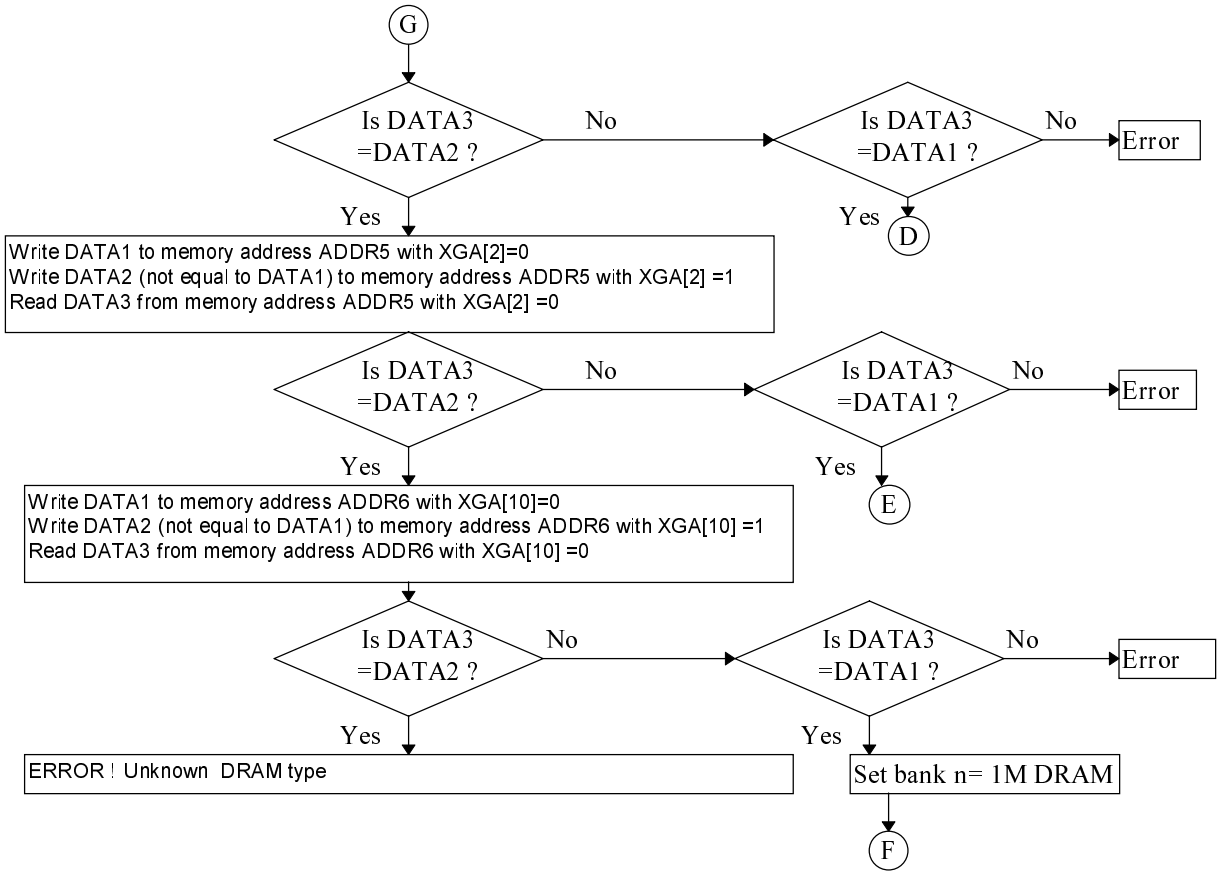


Figure 1-2. Memory Autosizing Flowchart - 2

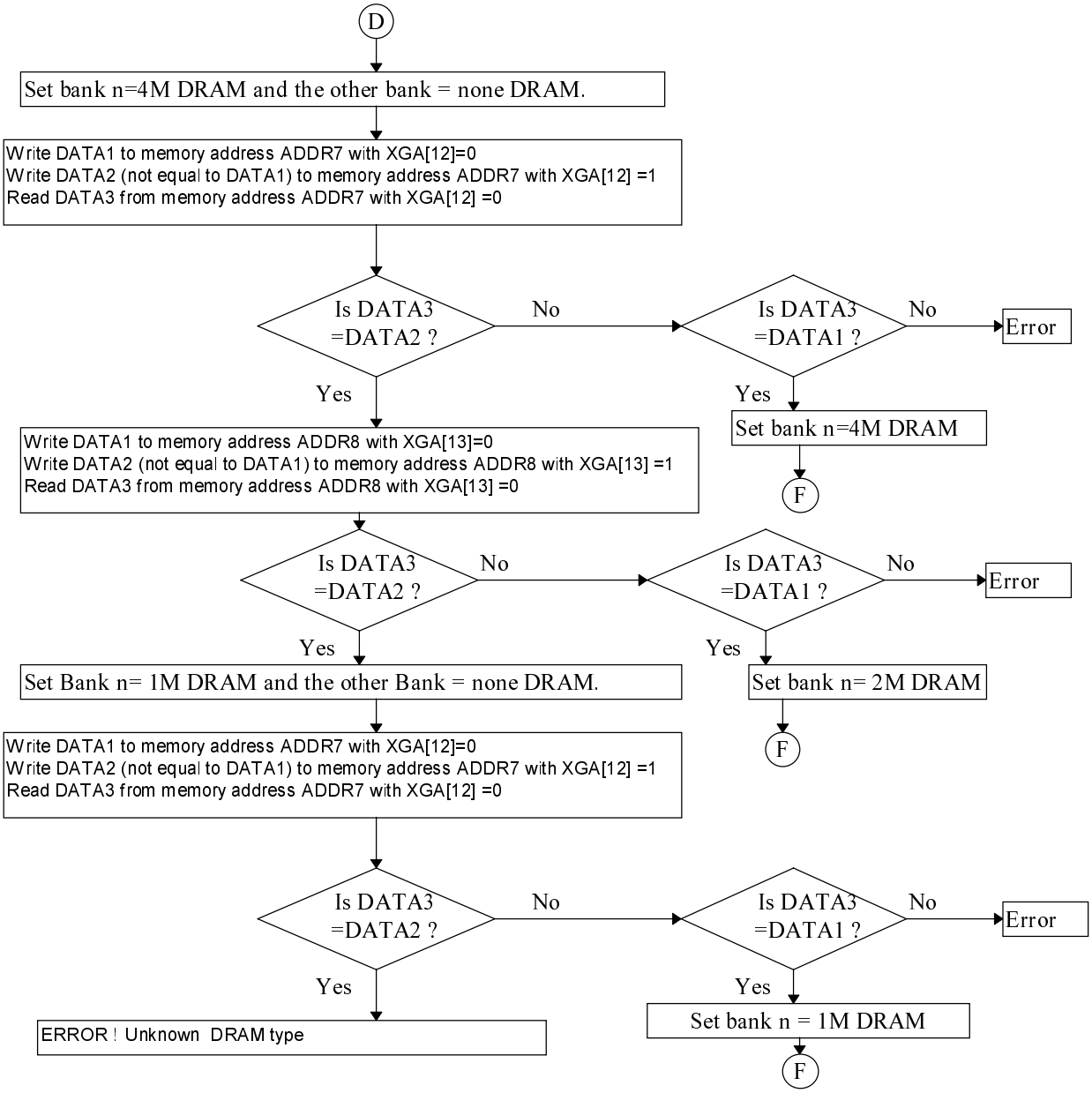


Figure 1-3. Memory Autosizing Flowchart - 3

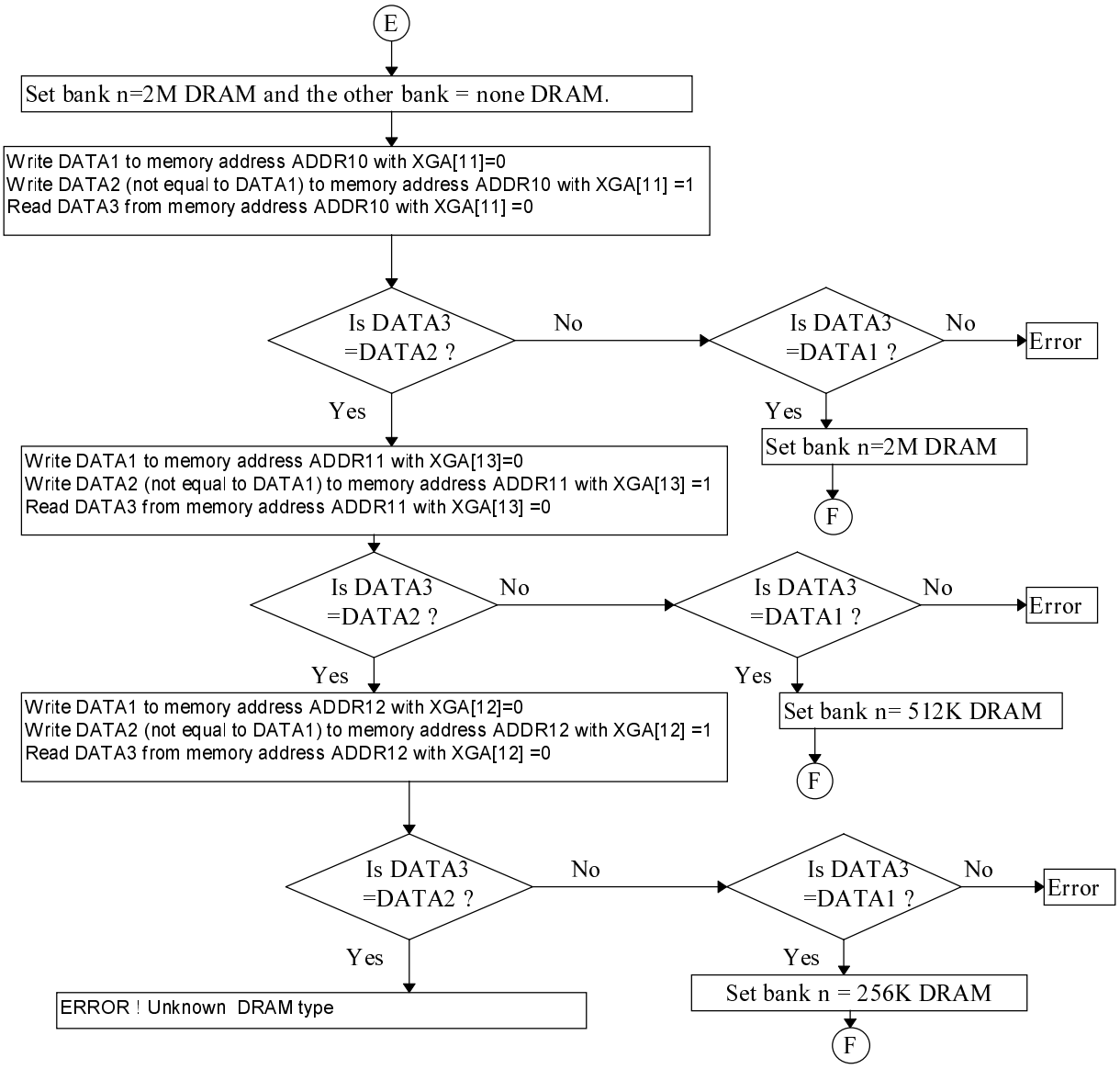


Figure 1-4. Memory Autosizing Flowchart - 4

Fig. 2-1
External Cache Auto-sizing
Flowchart 1 :
Main Procedure :

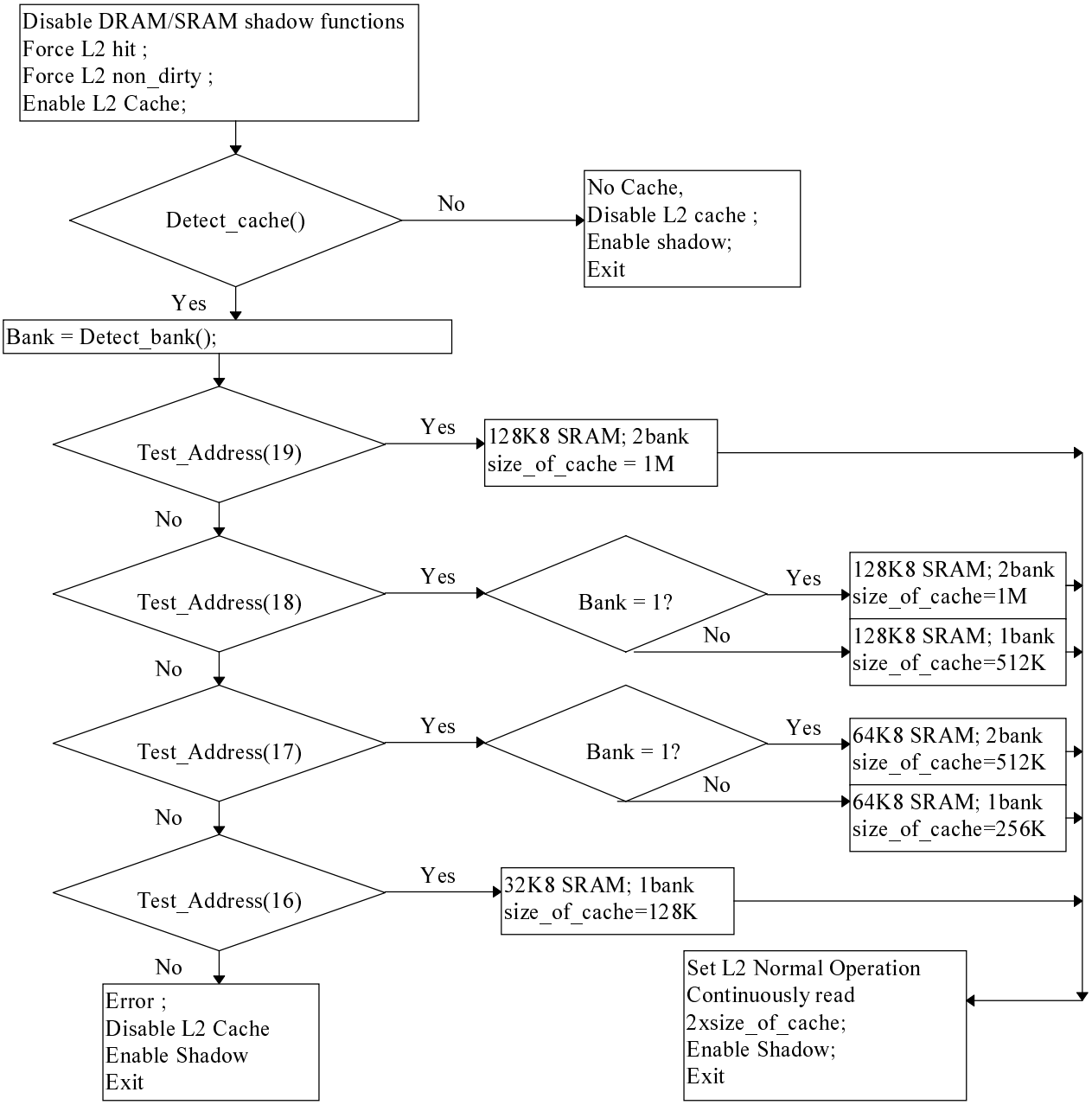


Fig. 2-2
External Cache Auto-sizing Flow chart 2 :

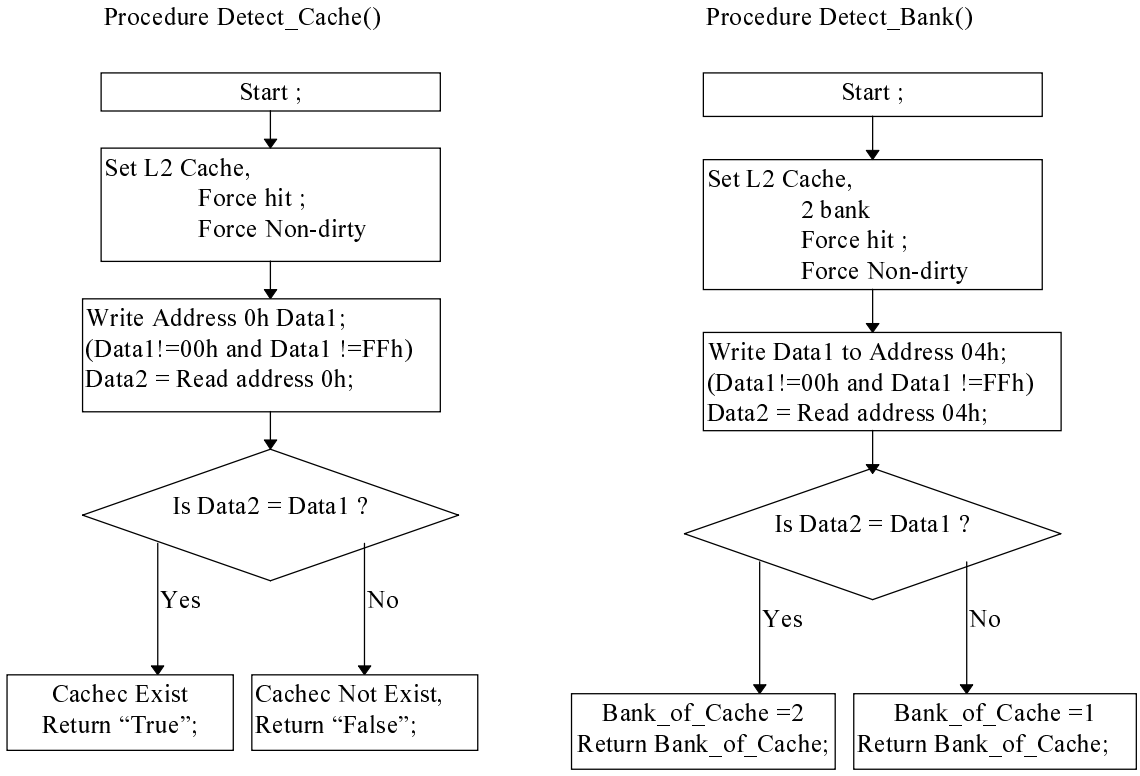


Fig. 2-3
External Cache Auto-sizing
Flowchart 3 :
Procedure Test_Address(i):

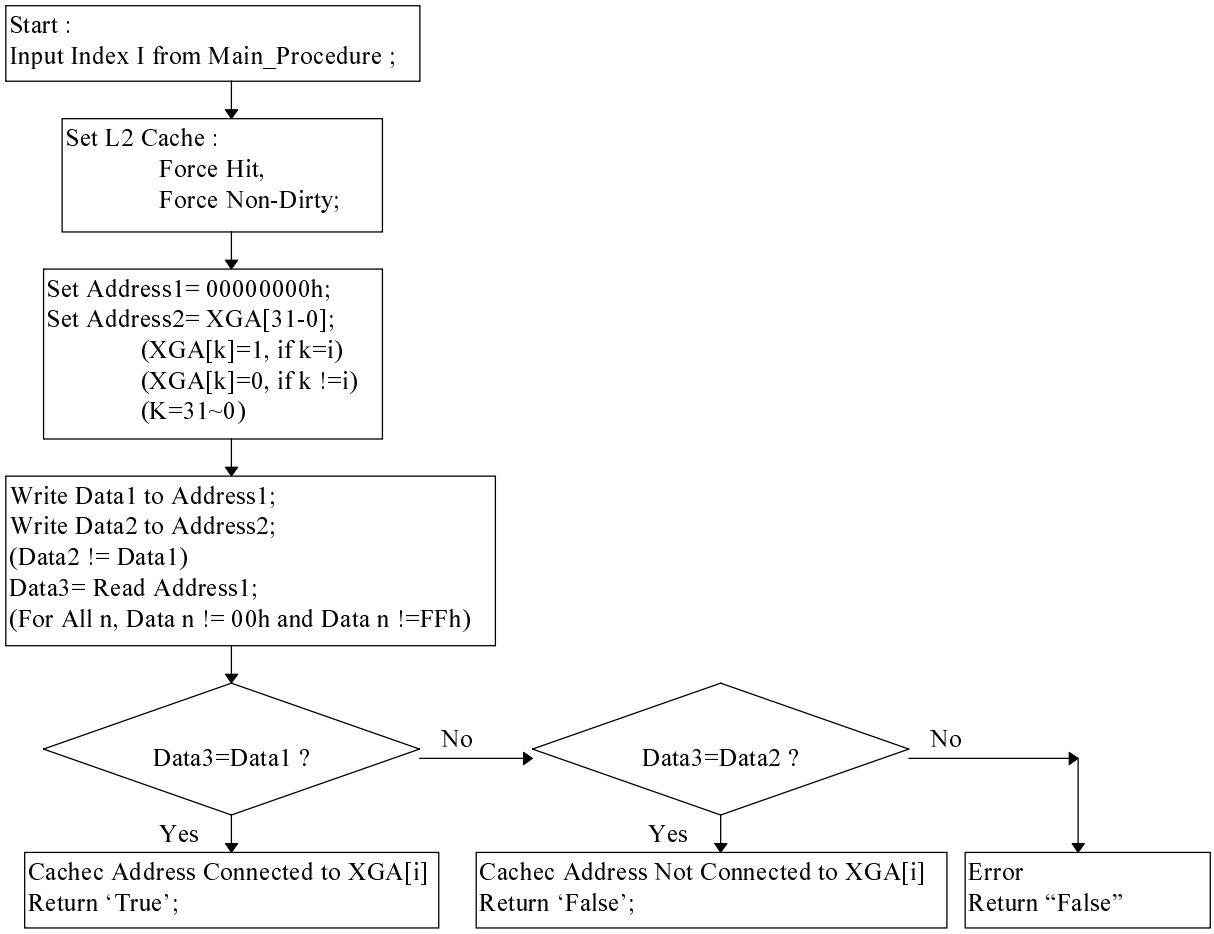


Fig. 3 M1489/M1487 SMI Control Flowchart

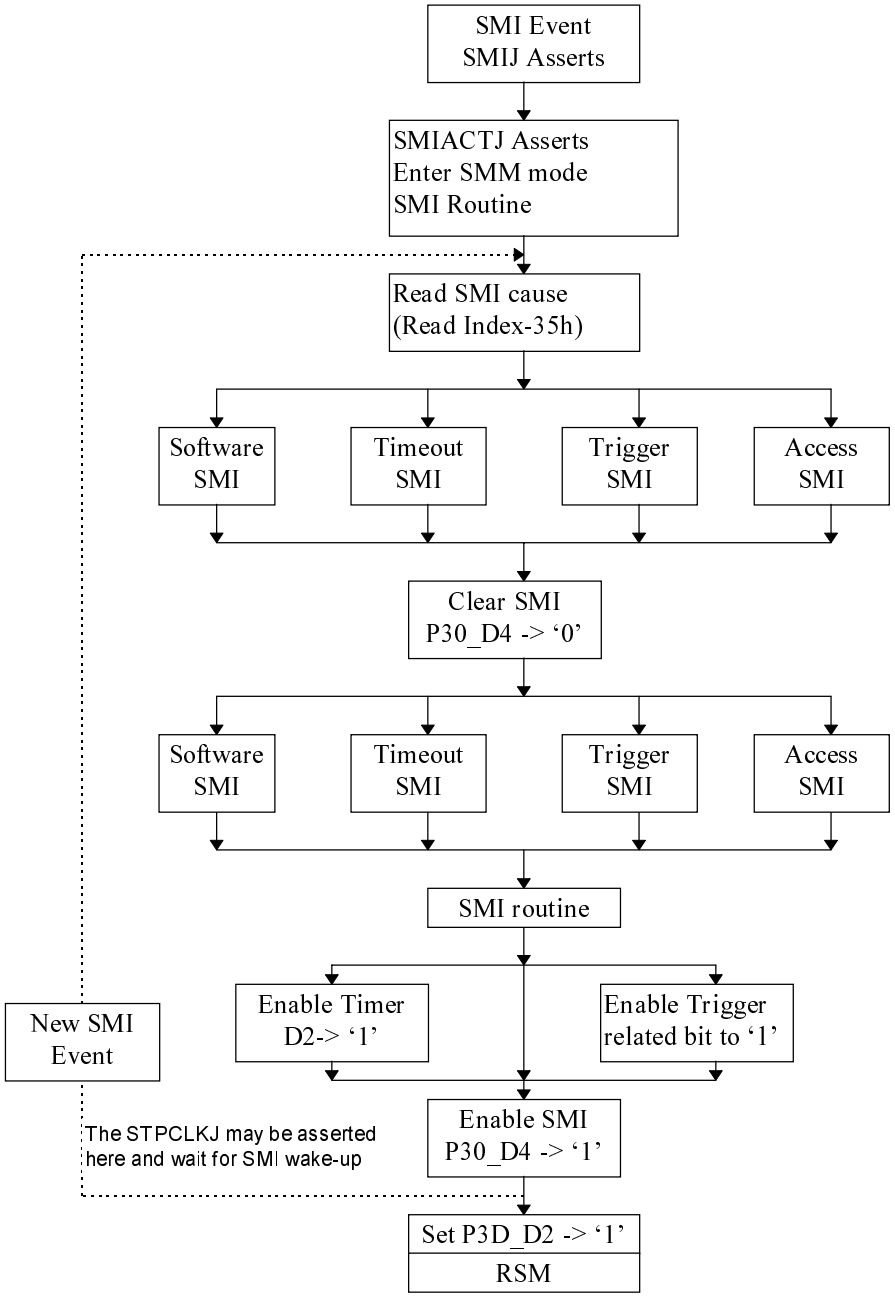
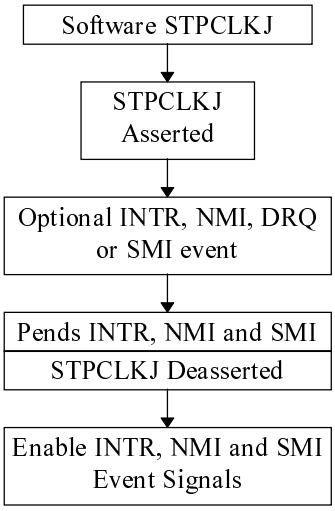
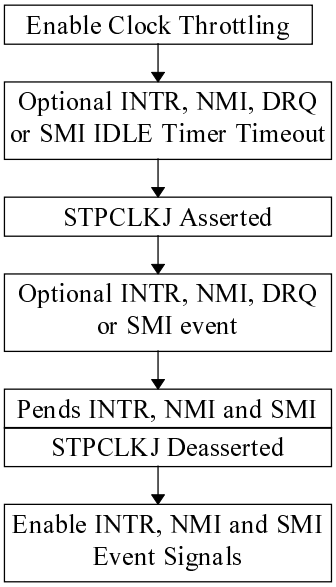


Fig. 4 M1489/M1487 STPCLKJ Control Flowchart





SMI Event and SMI Routine will disable Clock-Throttling Feature

Fig. 5-1 M1489/M1487 SMM Map Relocated Flowchart
Mapping Fig 2.3 & 2.4
Programming Flow

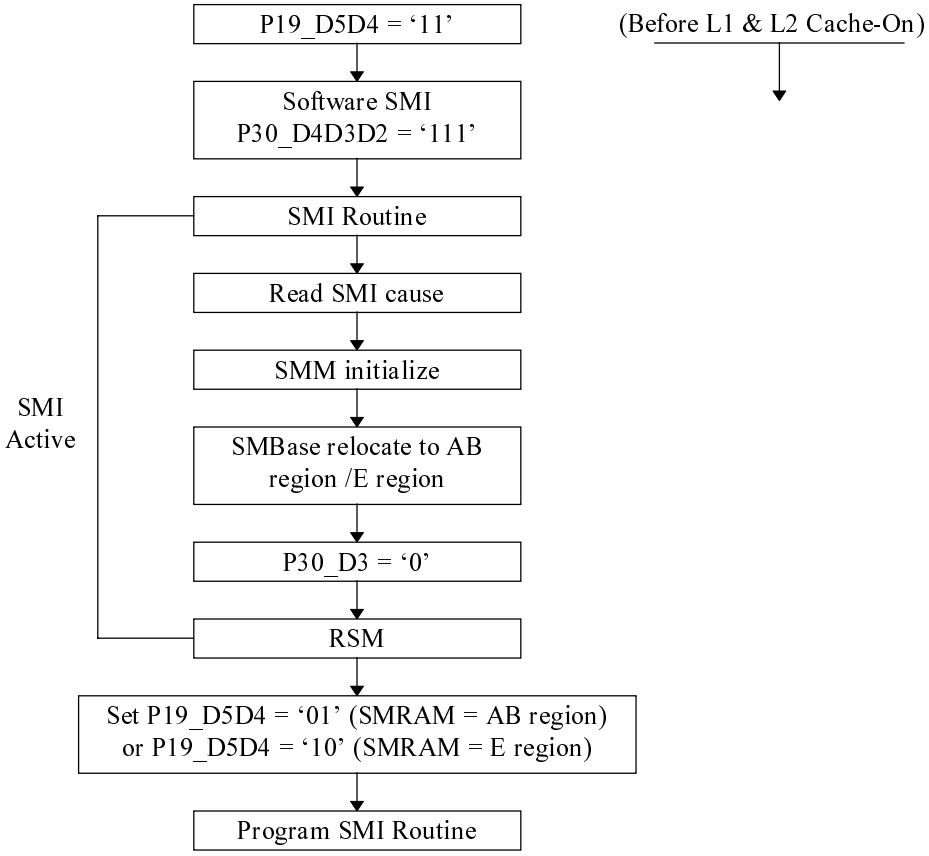
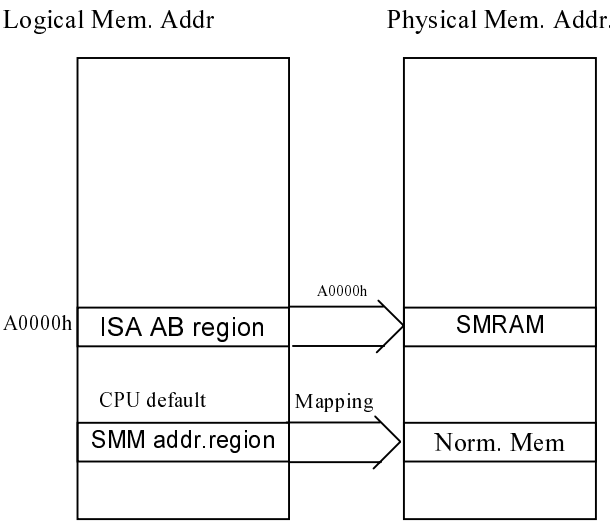
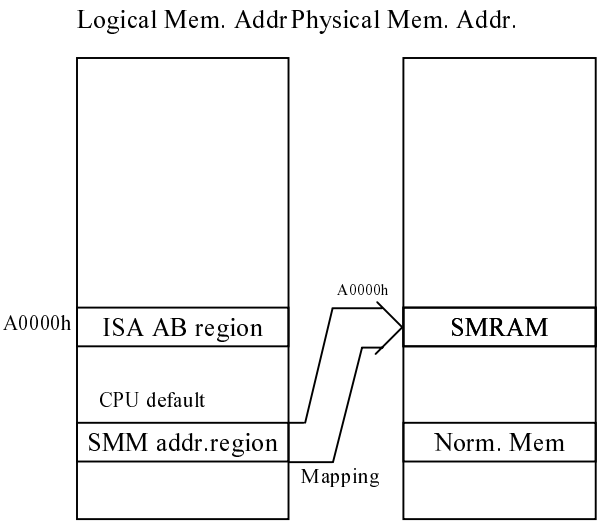


Fig. 5-2 SMM Mapping



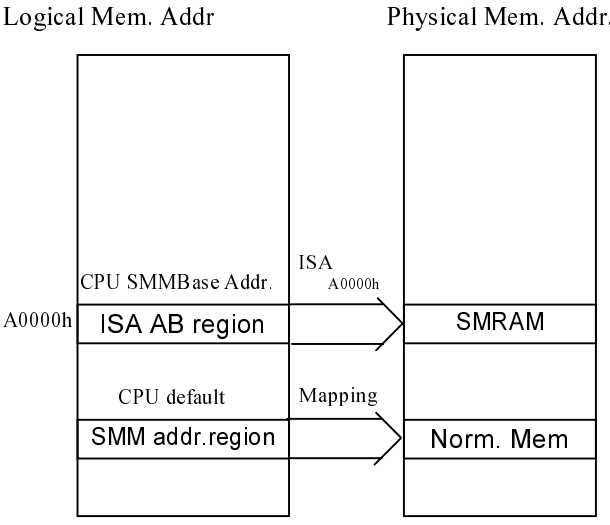
Mapping Fig.1.1

Condition:
Normal cycle
SMMBase=38000/68000
SMM Remap to AB region



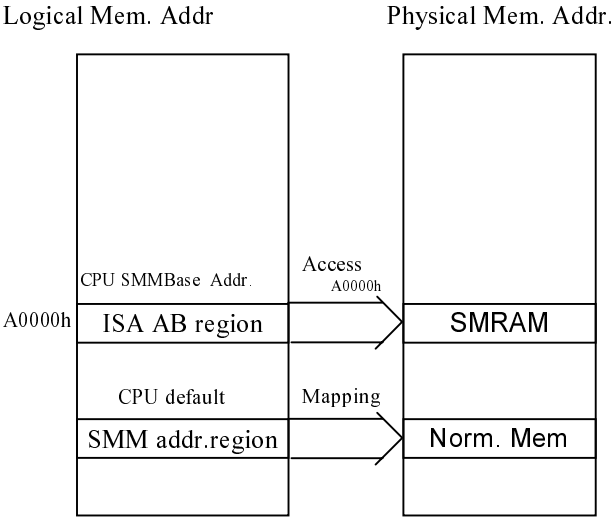
Mapping Fig.1.2

Condition:
Normal cycle
SMMBase=38000/68000
SMM Remap to AB region



Mapping Fig.1.3

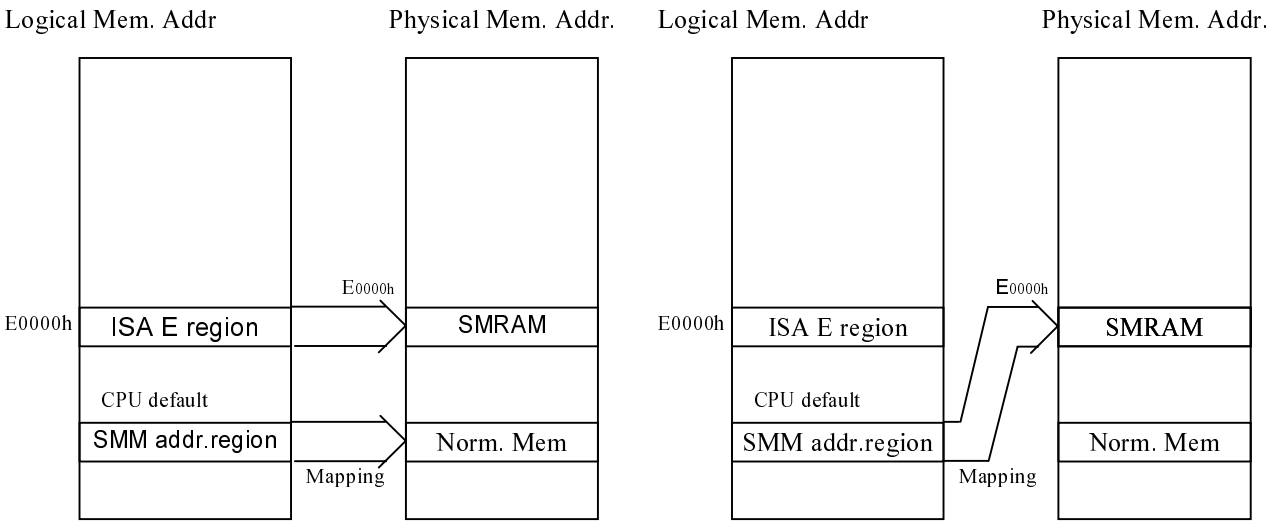
Condition:
Normal cycle
SMMBase=A0000~BFFFF



Mapping Fig.1.4

Condition :
SMM cycle
SMMBase=A0000~BFFFF

Fig. 5-3 SMM Mapping

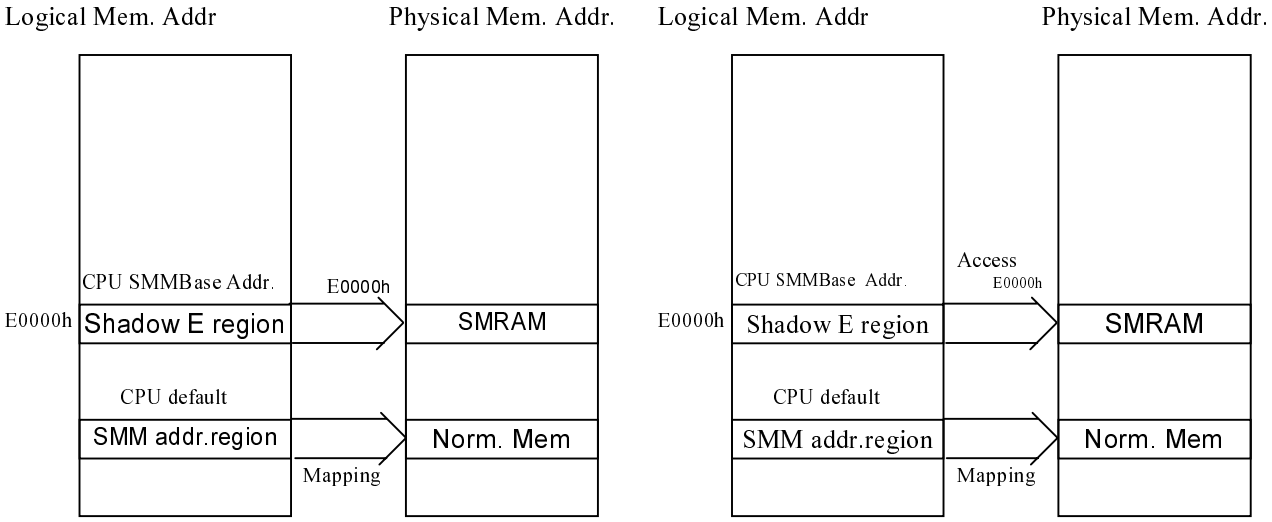


Mapping Fig.2.1

Condition:
Normal cycle
No shadow enable
CPU SMMBase= E region

Mapping Fig.2.2

Condition:
SMM cycle
No shadow enable
CPU SMMBase = E region



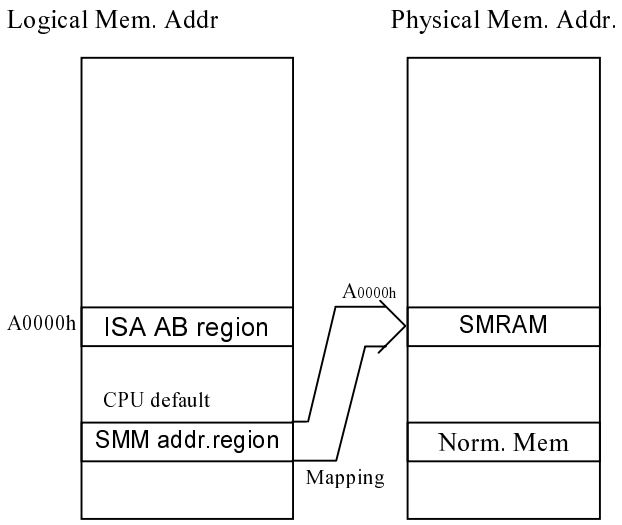
Mapping Fig.2.3

Condition:
Normal cycle
Shadow Enable
SMMBase=E region

Mapping Fig.2.4

Condition :
SMM cycle
Shadow enable
SMMBase=E region

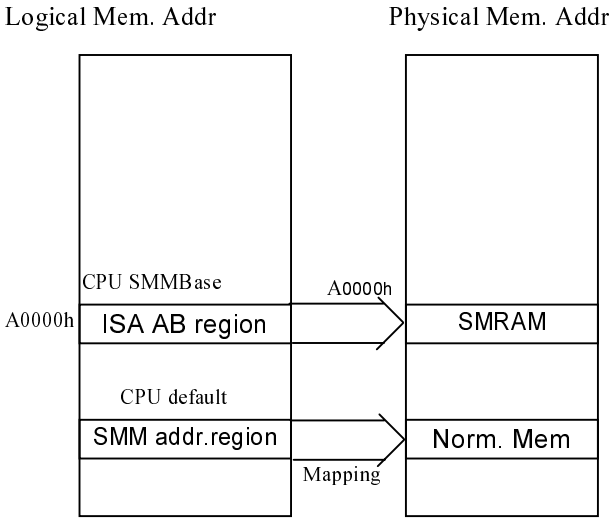
Fig. 5-4. SMM Mapping



Mapping Fig.3.1

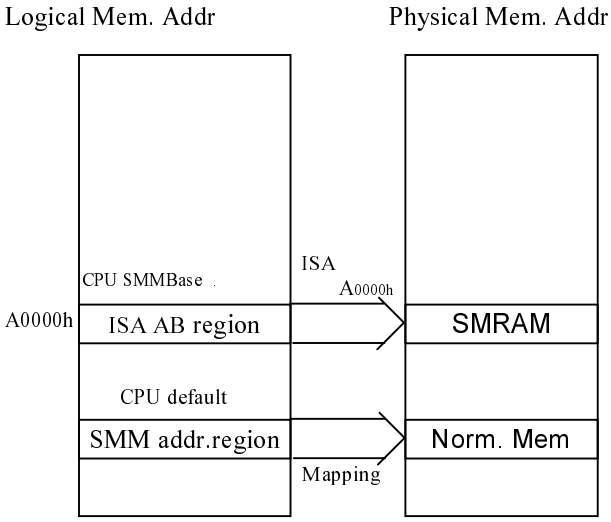
Condition: Normal or SMM cycle
CPU SMMBase=38000(68000 for AMD)
P19_D3 ='1'

Fig. 5-5. SMM Mapping



Mapping Fig.4.1

Condition: SMM cycle
CPU SMMBase=AB region
P19_D0 ='0'

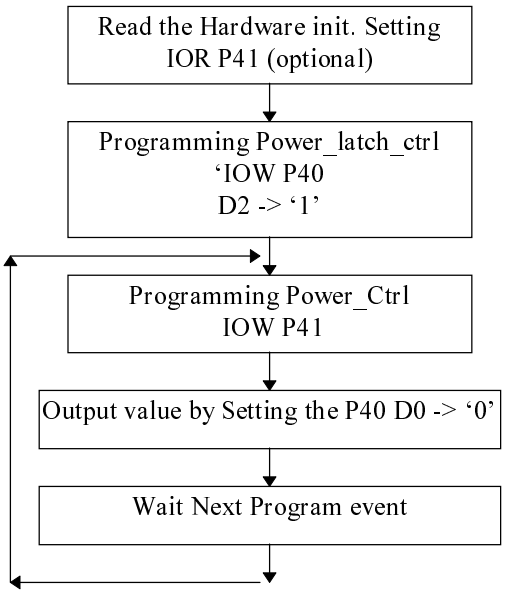


Mapping Fig.4.2

Condition : Normal or SMM cycle
CPU SMMBase=AB region
P19_D0 ='1'

Fig. 6 M1489/M1487 Power Control Signals Programming Flowchart

a. Latched Control for 8 Power Outputs



Latch Signal : CLKCTR
Latched Outputs : MA7~MA0

b. Level Control for CLKCTR output

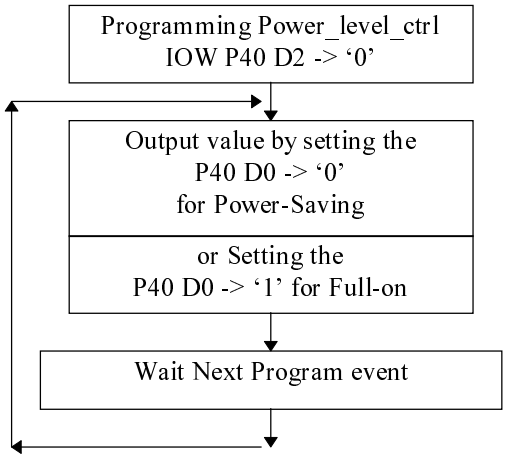
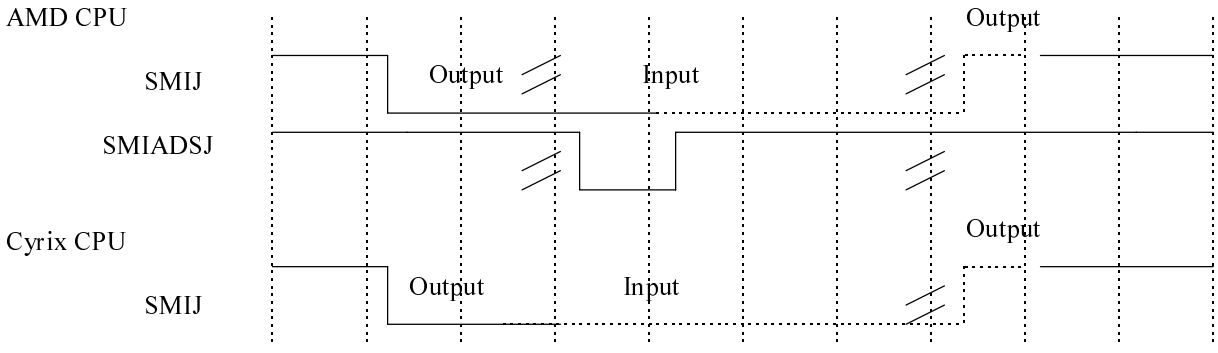


Fig. 7 M1489/M1487 SMI IO Timing Control

Intel CPU : M1489/M1487 SMIJ signal will always be output polarity



Section 7: Electrical Characteristics

7.1 M1489 AC Characteristics:

Table 7-1. M1489 AC Characteristics
Functional operating range : Vcc = 5V ± 0.5V; Tcase = 0 C to +70 C; C_L= 50pF unless otherwise specified.

Symbol	Parameter	Minimum	Maximum	Unit	Notes
	CPUCLK Frequency		50	MHz	Clock signal
	PCICLK Frequency		33	MHz	Clock signal
ts	RSTDRV setup time	5		ns	CPU side signals
th	RSTDRV hold time	2		ns	CPU side signals
tvd	GA[31],GA[26:2],BEJ[3:0] valid delay		13	ns	CPU side signals
tfd	GA[31],GA[26:2],BEJ[3:0] float delay		10	ns	CPU side signals
ts	GA[31],GA[26:2],BEJ[3:0] setup time	11		ns	CPU side signals
th	GA[31],GA[26:2],BEJ[3:0] hold time	6		ns	CPU side signals
tvd	GD[31:0] valid delay		13	ns	CPU side signals
tfd	GD[31:0] float delay		10	ns	CPU side signals
ts	GD[31:0] setup time	8		ns	CPU side signals
th	GD[31:0] hold time	6		ns	CPU side signals
ts	ADSJ,MIOJ,DCJ,WRJ setup time	11		ns	CPU side signals
th	ADSJ,MIOJ,DCJ,WRJ hold time	5		ns	CPU side signals
tvd	RDYOJ,BRDYOJ valid delay		10	ns	CPU side signals
tfd	RDYOJ,BRDYOJ float delay		8	ns	CPU side signals
ts	PCD setup time	11		ns	CPU side signals
th	PCD hold time	8		ns	CPU side signals
ts	LOCKJ,HITMJ setup time	11		ns	CPU side signals
th	LOCKJ,HITMJ hold time	8		ns	CPU side signals
tvd	BOFFJ valid delay		10	ns	CPU side signals
tfd	BOFFJ float delay		8	ns	CPU side signals
tvd	AHOLD valid delay		10	ns	CPU side signals
tfd	AHOLD float delay		8	ns	CPU side signals
tvd	EADSJ valid delay		10	ns	CPU side signals
tfd	EADSJ float delay		8	ns	CPU side signals
tvd	KENOJ valid delay		10	ns	CPU side signals
tfd	KENOJ float delay		8	ns	CPU side signals
tvd	RASJ[3:0] valid delay		14	ns	CPU side signals
tfd	RASJ[3:0] float delay		10	ns	CPU side signals
tvd	CASJ[3:0] valid delay		10	ns	CPU side signals
tfd	CASJ[3:0] float delay		8	ns	CPU side signals
tvd	MA[11:0] valid delay		14	ns	CPU side signals
tfd	MA[11:0] float delay		10	ns	CPU side signals
tvd	MWEJ valid delay		14	ns	CPU side signals
tfd	MWEJ float delay		10	ns	CPU side signals
tvd	COEJ[1:0] valid delay		10	ns	CPU side signals
tfd	COEJ[1:0] float delay		6	ns	CPU side signals
tvd	CWEJ[1:0] valid delay		10	ns	CPU side signals
tfd	CWEJ[1:0] float delay		6	ns	CPU side signals

Table 7-1. M1489 AC Characteristics (continued)

Symbol	Parameter	Minimum	Maximum	Unit	Notes
ts	CSJ[3:0]/PD[3:0] setup time	5		ns	CPU side signals
th	CSJ[3:0]/PD[3:0] hold time	3		ns	CPU side signals
tvd	CSJ[3:0]/PD[3:0] valid delay		10	ns	CPU side signals
tfd	CSJ[3:0]/PD[3:0] float delay		6	ns	CPU side signals
tvd	TAGWEJ valid delay		10	ns	CPU side signals
tfd	TAGWEJ float delay		6	ns	CPU side signals
ts	TAG[7:0] setup time	8		ns	CPU side signals
th	TAG[7:0] hold time	3		ns	CPU side signals
tvd	TAG[7:0] valid delay		10	ns	CPU side signals
tfd	TAG[7:0] float delay		10	ns	CPU side signals
tvd	A3I,A3II valid delay		10	ns	CPU side signals
tfd	A3I,A3II float delay		10	ns	CPU side signals
ts	SMIACKJ setup time	11		ns	CPU side signals
th	SMIACKJ hold time	5		ns	CPU side signals
tvd	CLEAROKJ valid delay		8	ns	Linkbus signals
tfd	CLEAROKJ float delay		6	ns	Linkbus signals
tvd	CMPSTJ valid delay		8	ns	Linkbus signals
tfd	CMPSTJ float delay		6	ns	Linkbus signals
ts	CMPGNTJ setup time	7		ns	Linkbus signals
th	CMPGNTJ hold time	3		ns	Linkbus signals
ts	IBCSTJ setup time	7		ns	Linkbus signals
th	IBCSTJ hold time	3		ns	Linkbus signals
	HDD[15:0],HDIORJ,HDIOWJ, HDIORDYJ, HDIO16J,HDCSJ[3:0] Supports through ATA PIO mode 3,4 harddisk				
ts	PAD[31:0],C_BEJ[3:0],PAR,STOPJ, FRAMEJ,TRDYJ,DEVSELJ,IRDYJ setup time	7		ns	PCI side signals
th	PAD[31:0],C_BEJ[3:0],PAR,STOPJ, FRAMEJ,TRDYJ,DEVSELJ,IRDYJ hold time	2		ns	PCI side signals
tvd	PAD[31:0],C_BEJ[3:0],PAR,STOPJ, FRAMEJ,TRDYJ,DEVSELJ,IRDYJ valid delay		10	ns	PCI side signals
tfd	PAD[31:0],C_BEJ[3:0],PAR,STOPJ, FRAMEJ,TRDYJ,DEVSELJ,IRDYJ float delay		8	ns	PCI side signals

Note: ts = setup time
th = hold time
tvd = valid delay time
tfd = float delay time

7.2 M1487 AC Characteristics

Table 7-2. M1487 AC Characteristics
Functional operating range : Vcc = 5V ± 0.5V; Tcase = 0 C to +70 C; CL= 50pF unless otherwise specified.

Symbol	Parameter	Minimum	Maximum	Unit	Notes
	CPUCLK Frequency		50	MHz	Clock signal
	PCICLK Frequency		33	MHz	Clock signal
	OSC Frequency		14.318	MHz	Clock signal
	ATCLK Frequency		12	MHz	Clock signal
	PWG Schmitt level trigger				Power signals
tvd	CPURST,SYSRST,SYSRSTJ valid delay		7	ns	CPU side signals
tvd	A20MJ,INTR,IGNNEJ,NMI,SMIJ,STPCLKJ valid delay		7	ns	CPU side signals
tfd	A20MJ,INTR,IGNNEJ,NMI,SMIJ,STPCLKJ float delay		3	ns	CPU side signals
ts	FERRJ setup time	8		ns	CPU side signals
th	FERRJ hold time	3		ns	CPU side signals
ts	IO16J,MEM16J,IOCHRDYJ,MASTERJ, IOCHCHJ,REFRESHJ setup time	10		ns	ISA side signals
th	IO16J,MEM16J,IOCHRDYJ,MASTERJ, IOCHCHJ,REFRESHJ hold time	5		ns	ISA side signals
tvd	ZMRJ,ZMWJ,IORJ,IOWJ valid delay		18	ns	ISA side signals
tfd	ZMRJ,ZMWJ,IORJ,IOWJ float delay		7	ns	ISA side signals
tvd	ZSMEMRJ,ZSMEMWJ valid delay		18	ns	ISA side signals
tfd	ZSMEMRJ,ZSMEMWJ float delay		7	ns	ISA side signals
ts	N0WSJ setup time	9		ns	ISA side signals
th	N0WSJ hold time	5		ns	ISA side signals
tvd	ZBALE,ZAEN,SBHEJ valid delay		18	ns	ISA side signals
tfd	ZBALE,ZAEN,SBHEJ float delay		6	ns	ISA side signals
tvd	LA[23:17],SA[19:0] valid delay		18	ns	ISA side signals
tfd	LA[23:17],SA[19:0] float delay		6	ns	ISA side signals
tvd	SD[15:0] valid delay		18	ns	ISA side signals
tfd	SD[15:0] float delay		6	ns	ISA side signals
ts	DRQ[7:5],DRQ[3:0] setup time	-		ns	ISA side signals
th	DRQ[7:5],DRQ[3:0] hold time	-		ns	ISA side signals
tvd	DACKJ[7:5],DACKJ[3:0] valid delay		10	ns	ISA side signals
tfd	DACKJ[7:5],DACKJ[3:0] float delay		6	ns	ISA side signals
ts	IRQ[15:14],IRQ[12:9],IRQ[7:3], IRQ[1],IRQ8J setup time	-		ns	ISA side signals
th	IRQ[15:14],IRQ[12:9],IRQ[7:3], IRQ[1],IRQ8J hold time	-		ns	ISA side signals
tvd	XBUSCSJ valid delay		6	ns	ISA side signals
tfd	XBUSCSJ float delay		4	ns	ISA side signals
tvd	RTCAS valid delay		6	ns	ISA side signals
tfd	RTCAS float delay		3	ns	ISA side signals
tvd	TC valid delay		11	ns	ISA side signals
tfd	TC float delay		6	ns	ISA side signals
tvd	SPEAK valid delay		10	ns	ISA side signals

Table 7-2. M1487 AC Characteristics (continued)

Symbol	Parameter	Minimum	Maximum	Unit	Notes
tfd	SPEAK float delay		6	ns	ISA side signals
	TURBO,EXTSMI valid pulse width	5		ms	
tvd	CPUSPD valid delay		10	ns	ISA side signals
tfd	CPUSPD float delay		6	ns	ISA side signals
tvd	CLKCTR valid delay		10	ns	ISA side signals
tfd	CLKCTR float delay		6	ns	ISA side signals
tvd	ENRTC/RTCCSJ valid delay		5	ns	ISA side signals
tfd	ENRTC/RTCCSJ float delay		3	ns	ISA side signals
ts	PREQJ[2:0] setup time	10		ns	PCI side signals
th	PREQJ[2:0] hold time	3		ns	PCI side signals
tvd	PGNTJ[2:0] valid delay		13	ns	PCI side signals
tfd	PGNTJ[2:0] float delay		7	ns	PCI side signals
ts	FRAMEJ,IRDYJ setup time	7		ns	PCI side signals
th	FRAMEJ,IRDYJ hold time	2		ns	PCI side signals
ts	INTJ[3:0] setup time	7		ns	PCI side signals
th	INTJ[3:0] hold time	2		ns	PCI side signals
ts	GA[17:2] setup time	7		ns	Linkbus signals
th	GA[17:2] hold time	3		ns	Linkbus signals
tvd	GA[17:2] valid delay		13	ns	Linkbus signals
tfd	GA[17:2] float delay		8	ns	Linkbus signals
ts	CLEAROKJ setup time	8		ns	Linkbus signals
th	CLEAROKJ hold time	3		ns	Linkbus signals
tvd	CMPGNTJ valid delay		8	ns	Linkbus signals
tfd	CMPGNTJ float delay		6	ns	Linkbus signals
ts	CMPSTJ setup time	8		ns	Linkbus signals
th	CMPSTJ hold time	3		ns	Linkbus signals
tvd	IBCSTJ valid delay		8	ns	Linkbus signals
tfd	IBCSTJ float delay		6	ns	Linkbus signals

M1487 RESET signals active timing definition

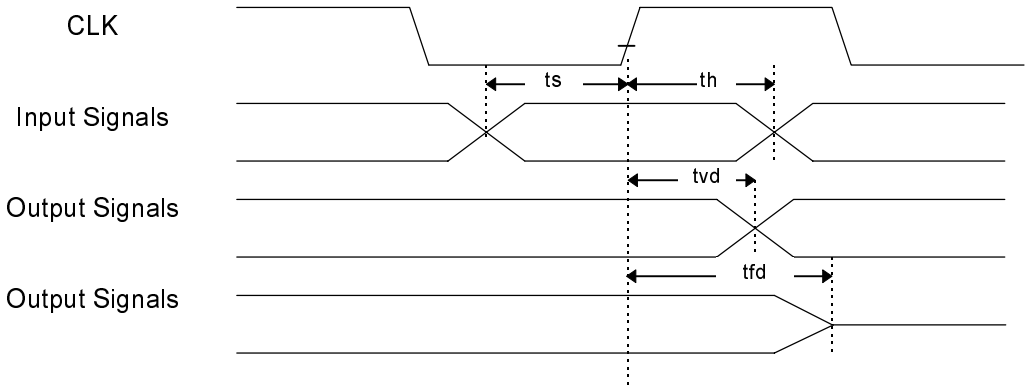
(1) CPURST(pin_20/M1487) will be driven active to about 2**19 ~ 2**20 OSC (pin_49/M1487) cycles (> 30 ms) after PWG(pin_13/M1487) is driven active (Power-on period).

(2) CPURST(pin_20/M1487) will be driven active to about 65 ~ 66 CPUCLK (pin_61/M1487) cycles in warm reset or soft reset periods.

(3) SYSRST(pin_63/M1487)/SYSRSTJ(pin_81/M1487) will be driven active to about 2**19 ~ 2**20 OSC(pin_49/M1487) cycles (> 30 ms) after PWG (pin_13/M1487) is driven active (Power-on period).

(4) Power-on Hardware Setup Signals Latch timing is defined about 2**13 ~ 2**14 OSC (pin_49/M1487) cycles (0.5 ms ~ 1 ms) after PWG (pin_13/M1487) is driven active (Power-on period).

M1489/M1487 AC Characteristics



Note : 1. For CPU side signals, CLK= CPUCLK (1)
2. For PCI side signals, CLK= PCICLK
3. For Linkbus side signals, CLK= PCICLK
4. For ISA side signals, CLK= ATCLK
5. Signal reference level : 1.5 V
6. Environment: Loading 50pF

7.3 DC Characteristics

Table 7-3 DC Characteristics

Symbol	Parameter	Minimum	Maximum	Units
V-IN-Hi	Input low voltage	-0.3	+0.8	V
V-IN-Hi	Input High voltage	2.0	Vcc+0.3	V
V-OUT-Low	Output low voltage		0.45	V
V-OUT-Hi	Output high voltage	2.4		V
ICC	Power supply current		200	mA*1
Ili	Input leakage current		±15	uA*2
Iih	Input leakage current		200	uA*3
Iil	Input leakage current		-200	uA*4
IoO	Output leakage current		±15	uA
Cin	Input capacitance		20	pF*5
Co	I/O or output capacitance		20	pF*5
Cclk	CLK capacitance		20	pF*5

Table 7-4 Absolute Maximum Ratings

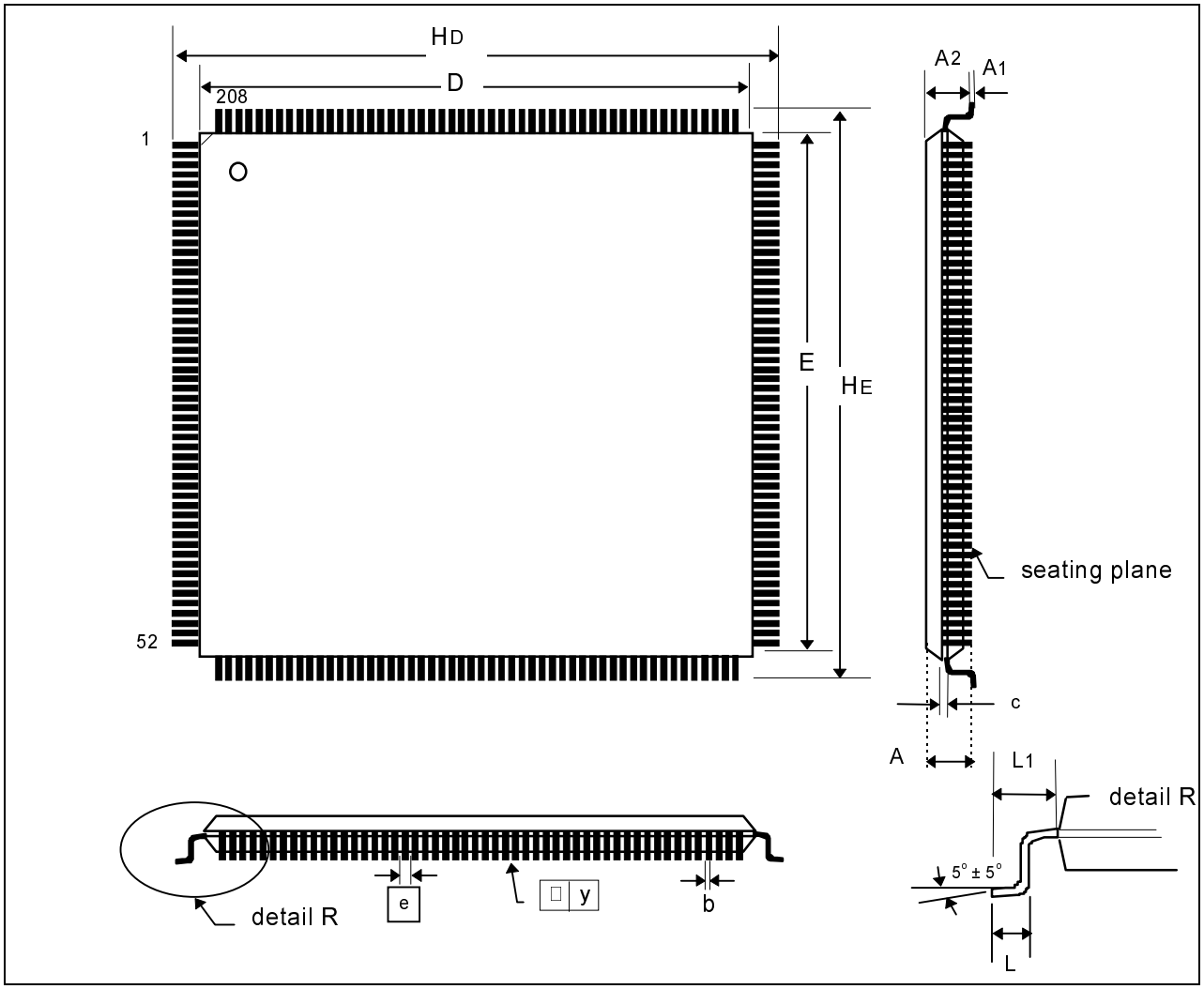
Symbol	Parameter	Minimum	Maximum	Unit
Vcc	Supply voltage	4.5	5.5	V*6
V-IN	Input voltage	-0.5	5.5	V
V-OUT	Output voltage	-0.5	5.5	V
Top	Operating temperature	0	70	C
Testing	Storage temperature	-40	125	C

Notes

*1 Typical supply current at 50-MHz
*2 For input without pull-ups or pull-downs, and if 0 £ V-IN £ Vcc
*3 For inputs with pull-downs and V-IN-Hi = 2.4V
*4 For inputs with pull-ups and V-IN-Low = 0.45V
*5 FC = 1-MHz and not 100% test
*6 This chip will not be damaged if the voltage is under the absolute minimum rating, but timing function is not guaranteed.

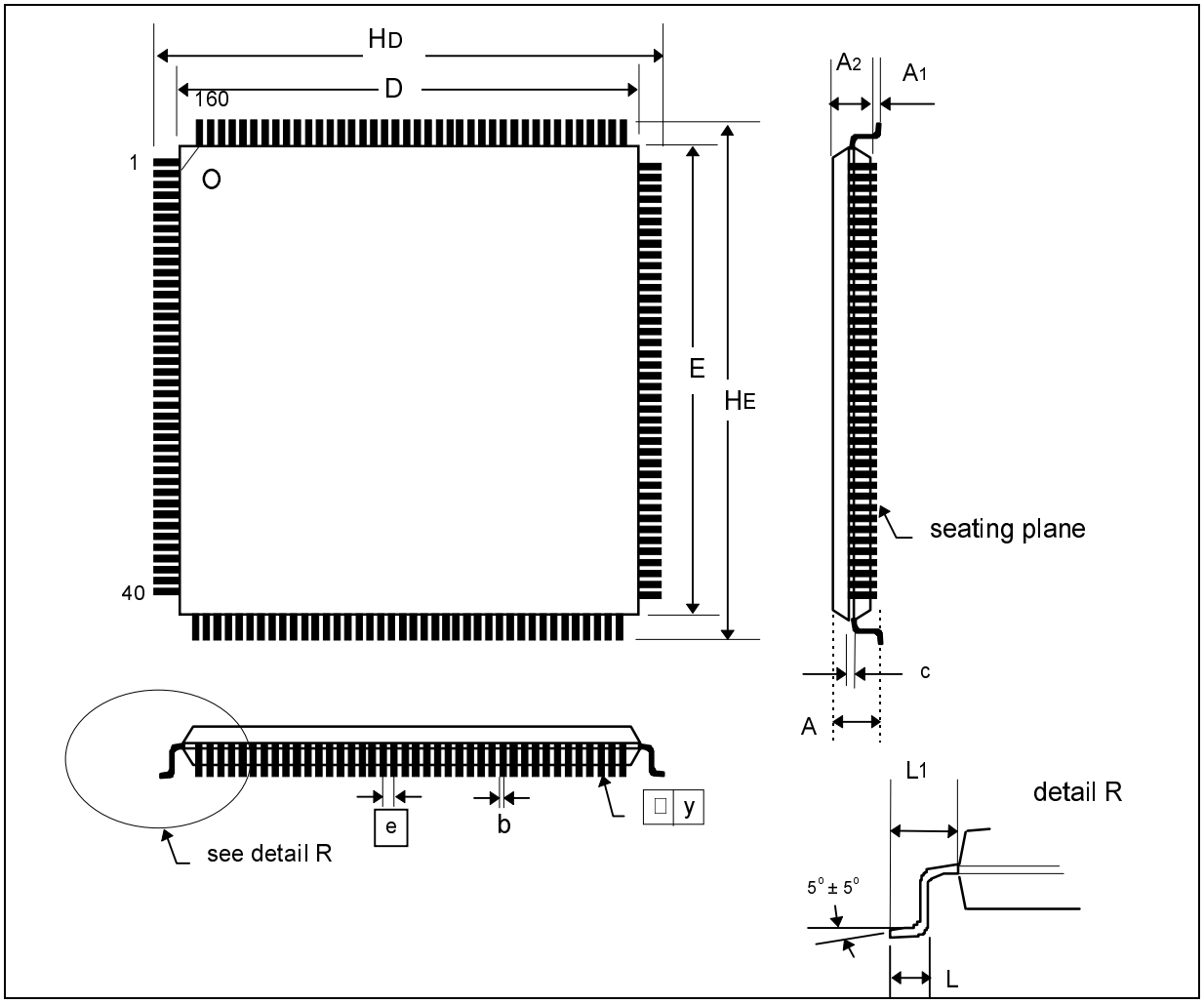
Section 8: Packaging Information

M1489: 208-pin PQFP



Symbol	Dimensions in Millimeters (nom)	Dimensions in Inches (nom.)
A	3.5 (max)	0.137 (max)
A_1	0.2 (min)	0.008 (min)
A_2	3.0	0.118
b	0.18	0.007
c	0.15	0.006
D	28.0	1.102
E	28.0	1.102
e	0.5	0.020
H_D	30.6	1.205
H_E	30.6	1.205
L_1	1.3	0.051
L	0.5	0.020
y	0.15 (max)	0.006 (max)

M1487: 160-pin PQFP



Symbol	Dimensions in Millimeters (nom.)	Dimensions in Inches (nom.)
A	3.5 (max)	0.138 (max)
A_1	0.20	0.008
A_2	3.20	0.126
b	0.30	0.012
c	0.15	0.006
D	28.0	1.102
E	28.0	1.102
e	0.65	0.026
H_D	32.0	1.260
H_E	32.0	1.260
L_1	2.01	0.079
L	0.8	0.031
y	0.10	0.004

Appendix A: BIOS Guide

1. Registers' Fixed Values

Index	Attribute	D7	D6	D5	D4	D3	D2	D1	D0
01h	R-Only	-	-	-	-	-	-	-	-
02h	R-Only	-	-	-	-	-	-	-	-
10h	R/W	-	-	-	-	-	-	-	-
11h	R/W		-	-	-	-	-	-	-
12h	R/W		-	-	-	-	-	-	-
13h	R/W		-	-	-	-	-	-	-
14h	R/W	1	-	-	-	-	-	-	-
15h	R/W	-	1	-	-	-	-	-	-
16h	R/W	-	-	-	-	-	-	-	-
17h	R/W	-	-	-	-	-	-	-	-
18h	reserved	-	-	-	-	-	-	-	-
19h	R/W	-	-	-	-	-	-	-	-
1Ah	R/W	-	1	-	1	-	-	-	-
1Bh	R/W	-	-	-	-	-	-	-	-
1Ch	R/W	-	-	-	-	-	-	-	-
1Dh	reserved	-	-	-	-	-	-	-	-
1Eh	R/W	-	-	-	-	-	-	-	-
1Fh	reserved	-	-	-	-	-	-	-	-
20h	R/W	-	-	-	-	-	-	-	-
21h	R/W	-	0	-	-	-	-	-	-
22h	R/W	-	-	-	-	-	1	-	-
23h	reserved	-	-	-	-	-	-	-	-
24h	reserved	-	-	-	-	-	-	-	-
25h	R/W	-	-	-	-	-	-	-	-
26h	R/W	-	-	-	-	-	-	-	-
27h	R/W	-	-	-	-	-	-	-	-
28h	R/W	-	-	-	-	-	-	-	-
29h	R/W	-	-	1	1	-	-	-	-
2Ah	R/W	-	1	-	-	-	-	-	-
2Bh	R/W	-	-	-	-	-	-	-	-
30h	R/W	-	-	-	-	-	-	-	-
31h	R/W	-	-	-	-	-	-	-	-
32h	R/W	-	-	-	-	-	-	-	-
33h	R/W	-	-	-	-	-	-	-	-
34h	R/W	-	-	-	-	-	-	-	-
35h	R/W	-	-	-	-	-	-	-	-
36h	R/W	-	-	-	-	-	-	-	-
37h	R/W	-	-	-	-	-	-	-	-
38h	R/W	-	-	-	-	-	-	-	-
39h	R/W	-	-	-	-	-	-	-	-
3Ah	R/W	-	-	-	-	-	-	-	-
3Bh	R/W	-	-	-	-	-	-	-	-
3Ch	R/W	-	-	-	-	-	-	-	-
3Dh	R/W	-	-	-	-	-	-	-	-
3Eh	reserved	-	-	-	-	-	-	-	-
3Fh	R-Only	-	-	-	-	-	-	-	-
40h	R/W	-	-	-	-	-	-	-	-
41h	R/W	-	-	-	-	-	-	-	-
42h	R/W	-	-	-	-	-	-	-	-
43h	R/W	-	-	-	-	-	-	-	-
44h	R/W	-	-	-	-	-	-	-	-
45h	R/W	1	-	-	-	-	-	-	-

2. Fixed Value Related to Different CPUs

a. If CPU is a Cyrix CPU except M1-SC, write 1 to Index-15h D0.

b. If CPU is a write back CPU (include Cyrix M7), write 1 to index-16h D2.

3. Chipset Registers' Setup Options

a. Auto Configuration Function: Disabled/Enabled

AT Bus Clock :	7.16	-- Index-29h D[2:0]=000
	CPU Bus Speed/3	-- Index-29h D[2:0]=001
	CPU Bus Speed/4	-- Index-29h D[2:0]=010
	CPU Bus Speed/5	-- Index-29h D[2:0]=011
	CPU Bus Speed/6	-- Index-29h D[2:0]=100
	CPU Bus Speed/8	-- Index-29h D[2:0]=101
DRAM Read Timing :	Slow	-- Index-1Bh D[1:0]=00
	Normal	-- Index-1Bh D[1:0]=01
	Faster	-- Index-1Bh D[1:0]=10
	Fastest	-- Index-1Bh D[1:0]=11
DRAM Write Timing :	Slow	-- Index-1Bh D[3:2]=00
	Normal	-- Index-1Bh D[3:2]=01
	Faster	-- Index-1Bh D[3:2]=10
	Fastest	-- Index-1Bh D[3:2]=11
SRAM Read Timin:	2-1-1-1	-- Index-15h D[5:4]=00 Index-16h D5=0
	3-1-1-1	-- Index-15h D[5:4]=01 Index-16h D5=0
	3-2-2-2	-- Index-15h D[5:4]=00 Index-16h D5=1
	4-2-2-2	-- Index-15h D[5:4]=01 Index-16h D5=1
SRAM Write Timing:	0 W	-- Index-16h D4=0
	1 W	-- Index-16h D4=1

b. Parity Check:	Disabled	-- Index-1Bh D5=0
	Enabled	-- Index-1Bh D5=1
c. Hidden Refresh:	Disabled	-- Index-12h D7=0
	Enabled	-- Index-12h D7=1
d. ISA I/O Recovery:	Disabled	-- Index-2Ah D[3:0]=0000
	Enabled	-- Index-2Ah D[3:0]=0101
e. CPU to PCI Write Buffe :	Disabled	-- Index-20h D4=0 D2=0 D1=0
	Enabled	-- Index-20h D4=1 D2=1 D1=1
Byte Merge:	Disabled	-- Index-20h D3=0
	Enabled	-- Index-20h D3=1
Fast Back_2_Back:	Disabled	-- Index-20h D5=0
	Enabled	-- Index-20h D5=1
f. VGA Locate Bus:	ISA	-- Index-20h D7=0 D6=0
	PCI	-- Index-20h D7=1 D6=0
g. PCI to DRAM Buffer:	Disabled	-- Index-22h D4=0 D3=0 D0=0
	Enabled	-- Index-22h D4=1 D3=1 D0=1
h. PCI VGA Colour Pallet Snoop :	Disabled	
	Enabled	
i. M1-SC Linear Wrapped Mode :	Disabled	-- Index-1Eh D6=0
	Enabled	-- Index-1Eh D6=1

4. IDE Option

Please follow the procedure listed below to program M1489 IDE:

a. Detect IDE PIO mode and how many IDEs in first and secondary channel first.

b. Then, use the following formula to calculate Data and Command Active and Recovery count and write the result to respective registers.

RA(Read Active Count) = {[Active time (ns) x CPU Bus Speed (MHz)] + 999} / 1000
RC(Read Cycle Count) = {[Cycle time (ns) x CPU Bus Speed (MHz)] + 999} / 1000
RR(Read Recovery Count) = RC - RA
WA(Write Active Count) = RA + 8
WR(Write Recovery Count) = RR + 8

The following table shows different Active and Cycle time for different PIO mode disks:

	Active time (16 Bits)(ns)	Active time (8 Bits)(ns)	Cycle time(ns)
Mode 0	165	290	600
Mode 1	125	290	383
Mode 2	100	290	240
Mode 3	80	80	180
Mode 4	70	70	120

IDE register index-02 (DBA: Data Byte Active Count for first channel) is decided by the value WA calculated by formula listed above using the 8 bits active time volume. If there are two devices attached in the first channel, use the worst (largest one) count.
IDE register index-25 (DBR: Data Byte Recovery Count for first channel) is decided by the value WR calculated by formula listed above using the 8 bits active time volume. If there are two devices attached in the first channel, use the worst (largest one) count.
IDE register index-03 (D0RA: Master Read Active Count for first channel) is decided by the value RA calculated by formula listed above using the 16 bits active time volume.
IDE register index-04 (D0WA: Master Write Active Count for first channel) is decided by the value WA calculated by formula listed above using the 16 bits active time volume.
IDE register index-05 (D1RA: Slave Read Active Count for first channel) is decided by the value RA calculated by formula listed above using the 16 bits active time volume.
IDE register index-06 (D1WA: Slave Write Active Count for first channel) is decided by the value WA calculated by formula listed above using the 16 bits active time volume.
IDE register index-26 (D0RR: Master Read Recovery Count for first channel) is decided by the value RR calculated by formula listed above using the 16 bits active time volume.
IDE register index-27 (D0WR: Master Write Recovery Count for first channel) is decided by the value WR calculated by formula listed above using the 16 bits active time volume.
IDE register index-28 (D1RR: Slave Read Recovery Count for first channel) is decided by the value RR calculated by formula listed above using the 16 bits active time volume.
IDE register index-29 (D1WR: Slave Write Recovery Count for first channel) is decided by the value WR calculated by formula listed above using the 16 bits active time volume.

IDE register index-2A (DBA: Data Byte Active Count for secondary channel) is decided by the value WA calculated by formula listed above using the 8 bits active time volume. If there are two devices attached in the secondary channel, use the worst (largest one) count.
IDE register Index-2F (DBR: Data Byte Recovery Count for secondary channel) is decided by the value WR calculated by formula listed above using the 8 bits active time volume. If there are two devices attached in the secondary channel, use the worst (largest one) count.
IDE register index-2B (D0RA: Master Read Active Count for secondary channel) is decided by the value RA calculated by formula listed above using the 16 bits active time volume.
IDE register index-2C (D0WA: Master Write Active Count for secondary channel) is decided by the value WA calculated by formula listed above using the 16 bits active time volume.
IDE register index-2D (D1RA: Slave Read Active Count for secondary channel) is decided by the value RA calculated by formula listed above using the 16 bits active time volume.
IDE register index-2E (D1WA: Slave Write Active Count for secondary channel) is decided by the value WA calculated by formula listed above using the 16 bits active time volume.
IDE register index-30 (D0RR: Master Read Recovery Count for secondary channel) is decided by the value RR calculated by formula listed above using the 16 bits active time volume.
IDE register index-31 (D0WR: Master Write Recovery Count for secondary channel) is decided by the value WR calculated by formula listed above using the 16 bits active time volume.
IDE register index-32 (D1RR: Slave Read Recovery Count for secondary channel) is decided by the value RR calculated by formula listed above using the 16 bits active time volume.
IDE register index-33 (D1WR: Slave Write Recovery Count for secondary channel) is decided by the value WR calculated by formula listed above using the 16 bits active time volume.

c. Please put some option in BIOS and they are described as follows:

(1) Local IDE Enable/Disable : This feature is determined by IDE register index-01 bit 0. Write 1 will enable M1489 local IDE. Another register value in index-01 is decided by CPU local bus speed. If speed is equal to or less than 33 MHz, write 07h to this register. If speed is greater than 33 Mhz, write 03h to this register.

(2) Local IDE Buffer Enable/Disable : When enable, write 1Fh to IDE register index-07 and enable the respective IDE disk buffer in IDE register index-0Ah bits 0-3. Bit 0 is for Master IDE disk in first channel, Bit 1 is for Slave IDE disk in first channel, bit 2 is for Master IDE disk in secondary channel, and bit 3 is for Slave IDE disk in secondary channel. Please do not enable the IDE disk buffer if the attached device is CD-ROM.

(3) Since some IDE can not run at the speed it claims. For example, some IDE can only run at PIO mode 2 even it claims itself a mode 3 disk. We suggest that put an option in BIOS which is Auto/Mode 0. If user chooses Auto, the IDE timing is determined by the IDE PIO mode. If user chooses Mode 0, BIOS just uses mode 0 timing to boot and performance will still be boosted by the IDE driver we support.

(4) Secondary channel Enable/Disable : Write 41h to IDE index-35h will disable the secondary IDE channel. Write 01h to IDE index-35h will enable the secondary IDE channel. When the secondary IDE channel is disabled, I/O port 170h-177h, 376h-377h and the interrupt 15 can be used by another device in PCI or ISA.

5. BIOS Setup for Safe and Optimum Value

CPU/Bus Speed	Intel/33, AMD/33, Cyrix/33 (*), Ti (*)		
Chipset Option	Safe	Optimum(1 Back)	Optimum (2 Back)
AT Bus Clock	7.16	33/4	33/4
DRAM Read Timing	Slow	Normal	Normal
DRAM Write Timing	Slow	Normal	Normal
SRAM Read Timing	4-2-2-2	2-1-1-1(**)	2-1-1-1(***)
SRAM Write Timing	1 W	0 W	0 W
CPU to PCI Write Buffer	Disabled	Enabled	Enabled
Byte Merge	Disabled	Disabled	Disabled
Fast B_2_B	Disabled	Disabled	Disabled
PCI to DRAM Buffer	Disabled	Enabled	Enabled
M1-SC Linear Wrapped Mode	Disabled	Disabled(****)	Disabled(****)

* Intel/33 includes DX-33, DX2-66, DX4-100, P24D-66, P24T-86(33/86).
AMD/33 includes DX2-66, DX4-100(SV8T), DX4 Plus-100(SV8B).
Cyrix/33 includes DX-33, DX2-66, DX4-100, M1SC-100(33/100).
Ti 486DX2-66 (Pin to pin compatible with Cyrix).

** It is strongly recommended to use -15ns SRAM to achieve 2-1-1-1 timing.
If you use -20ns tag SRAM and -20ns data SRAM, please change to 4-2-2-2.
If you use -15ns tag SRAM and -20ns data SRAM, please change to 3-2-2-2.

*** It is strongly recommended to use -15ns SRAM to achieve 2-1-1-1 timing. If you use -20ns tag SRAM, please change to 3-1-1-1. 2-bank SRAM configuration does not concern data SRAM speed (-15ns or -20ns).

**** M1SC-100 can enable this feature to boost performance.

CPU/Bus Speed	Intel/25 (*)		
Chipset Option	Safe	Optimum(1 Back)	Optimum(2 Back)
AT Bus Clock	7.16	25/3	25/3
DRAM Read Timing	Slow	Normal	Normal
DRAM Write Timing	Slow	Normal	Normal
SRAM Read Timing	4-2-2-2	2-1-1-1	2-1-1-1
SRAM Write Timing	1 W	0 W	0 W
CPU to PCI Write Buffer	Disabled	Enabled	Enabled
Byte Merge	Disabled	Disabled	Disabled
Fast B_2_B	Disabled	Disabled	Disabled
PCI to DRAM Buffer	Disabled	Enabled	Enabled
M1-SC Linear Wrapped Mode	Disabled	Disabled	Disabled

* Intel/25 includes DX-25, DX2-50, DX4-75, P24D-50, P24T-66(25/66).

CPU/Bus Speed	AMD/40, Cyrix/40, Ti/40, UMC/40 (*)		
Chipset Option	Safe	Optimum(1 Back)	Optimum(2 Back)
AT Bus Clock	7.16	40/5	40/5
DRAM Read Timing	Slow	Normal	Normal
DRAM Write Timing	Slow	Normal	Normal
SRAM Read Timing	4-2-2-2	4-2-2-2	4-2-2-2
SRAM Write Timing	1 W	0 W	0 W
CPU to PCI Write Buffer	Disabled	Enabled	Enabled
Byte Merge	Disabled	Disabled	Disabled
Fast B_2_B	Disabled	Disabled	Disabled
PCI to DRAM Buffer	Disabled	Enabled	Enabled
M1-SC Linear Wrapped Mode	Disabled	Disabled	Disabled

* AMD/40 includes DX2-80.
  Cyrix/40 includes DX-40, DX2-80.
  UMC/40 includes U5-40, U5-80.
  Ti 486DX2-80 (Pin-to-pin compatible with Cyrix).

CPU/Bus Speed	UMC/33 (*)		
Chipset Option	Safe	Optimum(1 Back)	Optimum(2 Back)
AT Bus Clock	7.16	33/4	33/4
DRAM Read Timing	Slow	Normal	Normal
DRAM Write Timing	Slow	Normal	Normal
SRAM Read Timing	4-2-2-2	3-1-1-1(**)	3-1-1-1(***)
SRAM Write Timing	1 W	0 W	0 W
CPU to PCI Write Buffer	Disabled	Enabled	Enabled
Byte Merge	Disabled	Disabled	Disabled
Fast B_2_B	Disabled	Disabled	Disabled
PCI to DRAM Buffer	Disabled	Enabled	Enabled
M1-SC Linear Wrapped Mode	Disabled	Disabled(****)	Disabled(****)

* UMC/33 includes U5-33, U5-66.

** It is strongly recommended to use -15ns SRAM to achieve 3-1-1-1 timing.
If you use -20ns tag SRAM and -20ns data SRAM, please change to 4-2-2-2.
If you use -15ns tag SRAM and -20ns data SRAM, please remain to 4-2-2-2.

*** 2-bank SRAM configuration does not concern data SRAM speed (-15ns or -20ns).

CPU/Bus Speed	M1SC/50 (*)		
Chipset Option	Safe	Optimum(1 Back)	Optimum(2 Back)
AT Bus Clock	7.16	50/6	50/6
DRAM Read Timing	Slow	Slow	Slow
DRAM Write Timing	Slow	Normal	Normal
SRAM Read Timing	4-2-2-2	4-2-2-2	4-2-2-2
SRAM Write Timing	1 W	0 W	0 W
CPU to PCI Write Buffer	Disabled	Enabled	Enabled
Byte Merge	Disabled	Disabled	Disabled
Fast B_2_B	Disabled	Disabled	Disabled
PCI to DRAM Buffer	Disabled	Enabled	Enabled
M1-SC Linear Wrapped Mode	Disabled	Disabled(**)	Disabled(**)

* M1-SC/50 includes M1SC-50(50/100).
** M1-SC can enable this feature to boost performance.

The following tables are used for a MB that does not implement 2nd level cache and uses EDO DRAMs. The table only lists the optimum option for DRAM timing, the others are the same as the tables listed above.

EDO DRAM Timing	-70ns			
CPU Bus Speed	25	33	40	50
DRAM Read Timing	Fastest	Faster	Faster	Faster
DRAM Write Timing	Fastest	Fastest	Faster	Faster
SRAM Read Timing	2-1-1-1	2-1-1-1	2-1-1-1	4-2-2-2
SRAM Write Timing	0 W	0 W	0 W	0 W

EDO DRAM Timing	-60ns			
CPU Bus Speed	25	33	40	50
DRAM Read Timing	Fastest	Fastest	Faster	Faster
DRAM Write Timing	Fastest	Fastest	Faster	Faster
SRAM Read Timing	2-1-1-1	2-1-1-1	2-1-1-1	4-2-2-2
SRAM Write Timing	0 W	0 W	0 W	0 W

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