Giantplus
Technology

APPROVAL SHEET
承　　認　　書

Customer 客戶名稱	金遠見
Part No. 產品型號	GPM940B0
Product type 產品內容	3.0” TFT module: Transmissive Type, Positive mode , Graphic 960(RGB)*240 Delta type
RoHS	☐ Non-compliance ■ Compliance
Remarks 備註欄	

☐Preliminary Specification　暫行規格
■Final Specification　正式規格

Signature by Customer：
客戶確認簽章：

Issued by QA	Checked by QA		Checked by PM	Approved By QA	Approved By BU

RoHS COMPLIANT

Giantplus Technology

Specification of LCD Module

Product No.: GPM940B0

Issue date: 2009/2/18

Giantplus Technology Co., LTD

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1. GENERAL DESCRIPTION

GPM940B0 is a trans-missive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver ICs, FPC, Bezel and a backlight unit.

2. FEATURES

Display Mode	Transmissive Type
	TFT LCD, Positive mode
Screen Size	3.0 inch
Display Format	Graphic 960(RGB)*240 Delta type
Color	16.7M color
Input Data	8-bit RGB(Note1)
Interface	Digital RGB
Backlight Color	White (LED*2)
Viewing Direction	6 O'clock

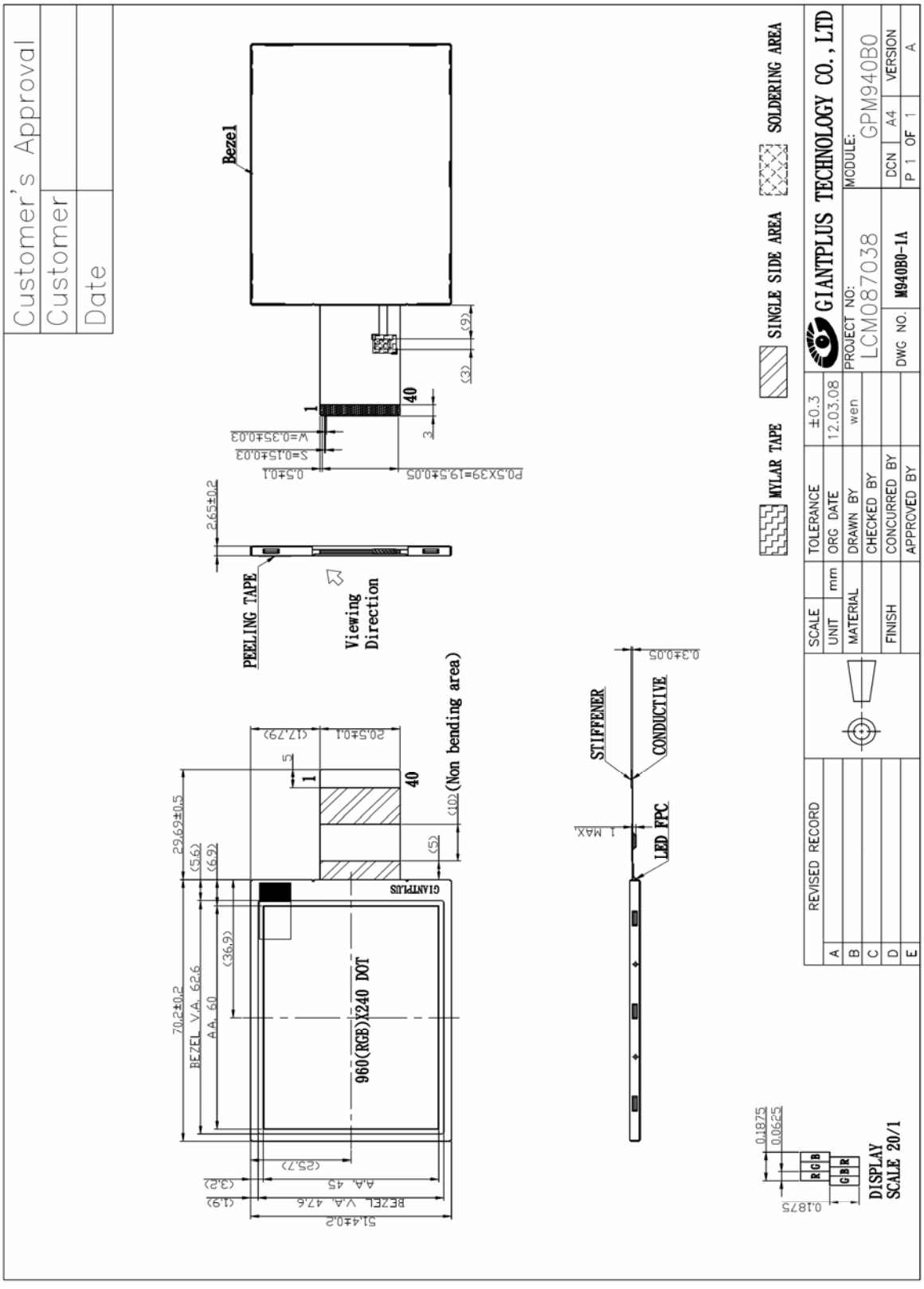
Note1：Input data including 8-bit RGB/ 8-bit Dummy RGB/ CCIR 601/ CCIR 656 For this IC

3. MECHANICAL SPECIFICATION

Item	Specifications	Unit
Dimensional outline	70.2 (W)×51.4(H) *×2.65(D)	mm
Resolution	960(R, G, B)×240	dot
Active area	60.0 (W)× 45.0 (H)	mm
Dot pitch	0.0625(W)×0.1875 (H)	mm

＊ Without FPC

4. MECHANICAL DIMENSION



5. MAXIMUM RATINGS

If the operating condition exceeds the following absolute maximum ratings, the TFT LCD module may be damaged permanently. PGND=VSS=0V,Ta=25°C

Item	Symbol	Values		Unit	Condition
		Min.	Max.		
Power voltage	VDD	-0.5	3.6	V	
	PVDD	-0.5	3.6	V	
Input signal voltage	VCOM	-2.9	5.2	V	
Digital Input Voltage	V_{IN}	-0.3	VDD+0.3	V	
Storage Temperature	T_{ST}	-30	80	°C	
Operating Temperature (Ambient Temperature)	T_{OP}	-20	70	°C	
Maximum clock frequency	Fmax	---	30	MHz	
Humidity	-	-	90	%RH	Note1

Note1: $T_A \leqq 40℃$ Without dewing

6. ELECTRICAL CHARACTERISTIC

a. Typical operating conditions

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Supply Voltage for Source Driver		VDD	3.0	3.3	3.6	V	
Supply Voltage for Gate Driver		PVDD	3.0	3.3	3.6		
	H level	VGH	14	18	19.5	V	Note6-1
	L Level	VGL	-7.5	-6	-4	V	Note6-1
Digital input Voltage	H level	V_{IH}	0.7VDD	-	VDD	V	
	L Level	V_{IL}	0	-	0.3VDD	V	
Digital output t Voltage	H level	V_{OH}	VDD-0.4	-	VDD	V	
	L Level	V_{OL}	0	-	VDD+0.4	V	
VCOM		V_{COMAC}	-	+4.4	+4.8	Vp-p	AC Component of VCOM
		V_{COMDC}	-	0.68	-	V	

Note6-1: VGH and VGL supplied by internal setup-up circuit

b. Current consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Current for FOG	IDD	VDD=+3.3V	9	13	mA	Note1
Current for LCM	PIDD	PVDD1=+3.3V	35.0	70.0	mA	Note2

Note 1:FOG means LCM without B/L unit.

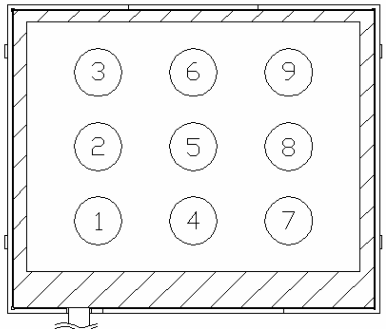
Note 2:The test condition is by reference application note as below

7. BACKLIGHT CHARACTERISTIC

7.1. Characteristic

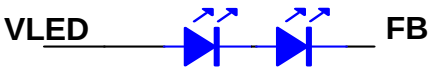
Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
LED Voltage	VLED	5.4	-	7.4	V	
LED Current	I_F	-	25	-	mA	2pcs LED
Feed back voltage	V_{FB}		0.6		V	

7.2. Lightguide Specification



a. Test Instrument: BM-7 (Distance =500mm; Field = 1°)

b. Light Source: LED * 2 (White)



c. Conditions: IF =25 mA,

d. Measure Brightness: 1 ~ 9

e. Uniformity = (Min. Brightness / Max. Brightness)*100%

f. Uniformity ≧ 70%

8. MODULE FUNCTION DESCRIPTION

8.1. PIN Description

Pin	Symbol	I/O	Function	Remark
1	VCOM	I	Common electrode driving voltage	Note 8-1
2	CS	I	Serial command enable-	
3	SDA	I	Serial command data input	
4	SCL	I	Serial command clock input	
5	HSYNC	I	Horizontal sync input	Note 8-6
6	VSYNC	I	Vertical sync input	Note 8-7
7	DCLK	I	Data clock input	Note 8-8
8	D7	I	Data input :MSB	
9	D6	I	Data input	
10	D5	I	Data input	
11	D4	I	Data input	
12	D3	I	Data input	
13	D2	I	Data input	
14	D1	I	Data input	
15	D0	I	Data input	
16	DGND	P	Ground terminal in the logic circuit.	
17	VDD	P	System Power	Note 8-3
18	VDDIO	P	Digital voltage input	
19	DVDD	C	Charge Pump Power GND	Note 8-2
20	V1	C	Charge Pump Power GND	
21	V2	C	Charge Pump Power GND	
22	V3	C	Charge Pump Power GND	
23	V4	C	Charge Pump Power GND	
24	VDD2	C	Charge Pump Power GND	
25	V5	C	Charge Pump Power GND	
26	V6	C	Charge Pump Power GND	
27	VDD3	C	Charge Pump Power GND.	
28	VDD5	C	Charge Pump Power GND.	Note 8-2
29	V7	C	Charge Pump Power GND.	
30	V8	C	Charge Pump Power GND.	
31	VGH	C	Serial communication clock input	
32	VGL	C	Horizontal sync input	
33	AGND	P	Ground terminal in the Analog circuit.	

Pin	Symbol	I/O	Function	Remark
34	FRP	O	Frame polarity output for VCOM	
35	COMDC	O	VCOM DC voltage output pin	
36	VCAC	C	Power setting	Note 8-2
37	DRV	O	VLED boost transistor for VCOM AC	Note 8-4
38	VLED	P	LED power anode	
39	FB	P	LED power cathode	Note 8-5
40	VCOM	I	Common electrode driving voltage	Note 8-1

I: Input O: Output P: Power I/O: Serial communication data input/output C: Capacitor

Note 8-1:VCOM=+4.8 Vp-p.(Typ.)

Note 8-2: The external capacitor is required on those pins as following.

Symbol	Capacitor No.	Part standard		Notes
		Capacitance	Voltage	
VGH	C11	≧4.7uF	25V over	
VGL	C12	≧4.7uF	16V over	
VCAC	C10	≧4.7uF	10V over	
DVDD	C6	≧4.7uF	6.3V over	
VDD/AVDD	C5	≧4.7uF	6.3V over	
C1P	C1	≧2.2uF	10V over	
C1M				
C2P	C2	≧2.2uF	10V over	
C2M				
C3P	C3	≧2.2uF	16V over	
C3M				
C4P	C4	≧2.2uF	16V over	
C4M				
VINT1	C7	≧4.7uF	10V over	
VINT2	C8	≧4.7uF	16V over	
VINT3	C9	≧4.7uF	25V over	
FRP/VCOMDC	C13	≧4.7uF	10V over	

Note 8-3: VDD, VDDIO=+3.3V (Typ.)

Note 8-4: Outputs the control signal of switching regulator for LED. Duty cycle varies according to FB input voltage

Note 8-5: Feedback signal of switching signal for LED. It controls DRV output duty cycle with 0.6V input level sense.

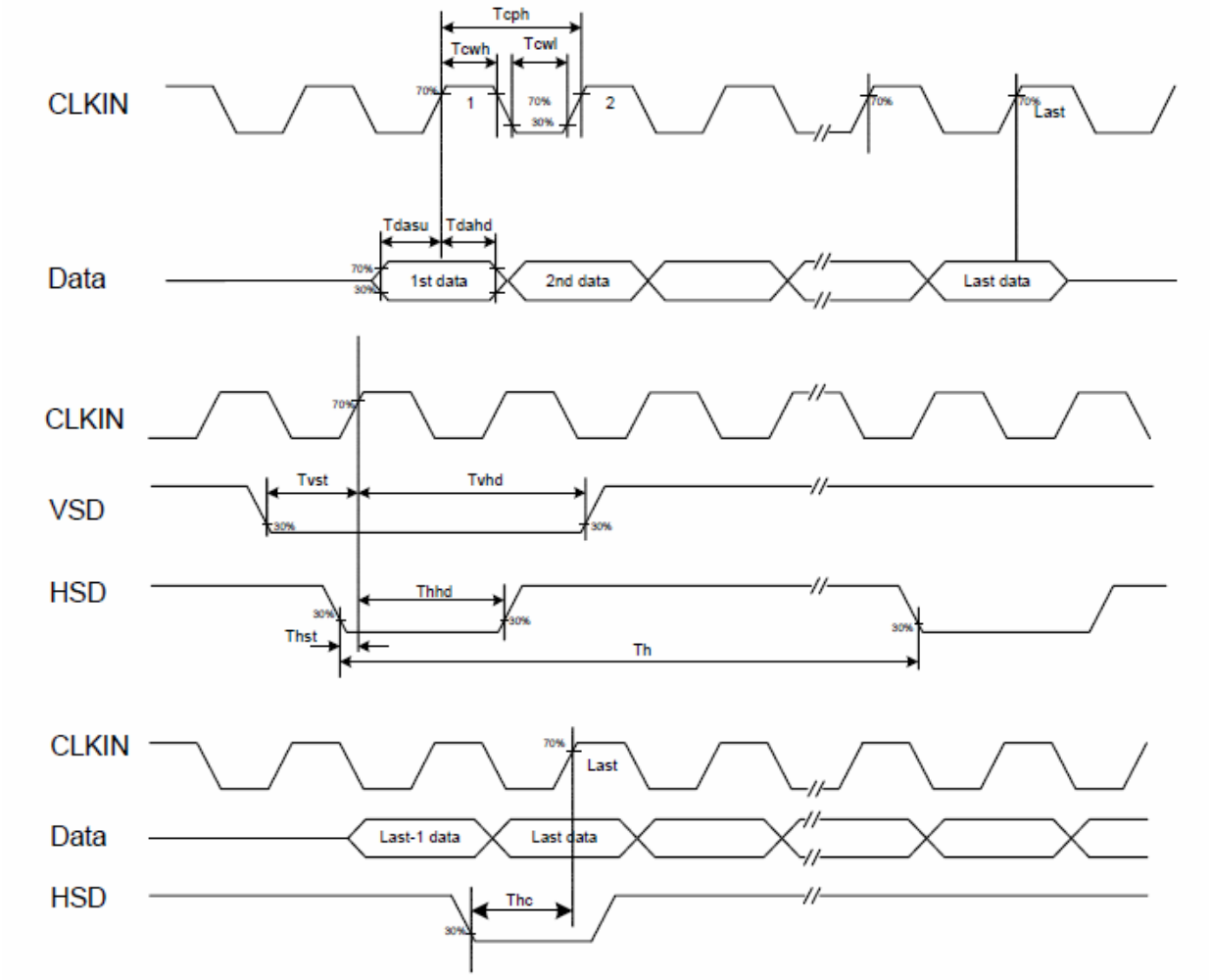
Note 8-6: Horizontal sync signal, it is a “Low “active signal.

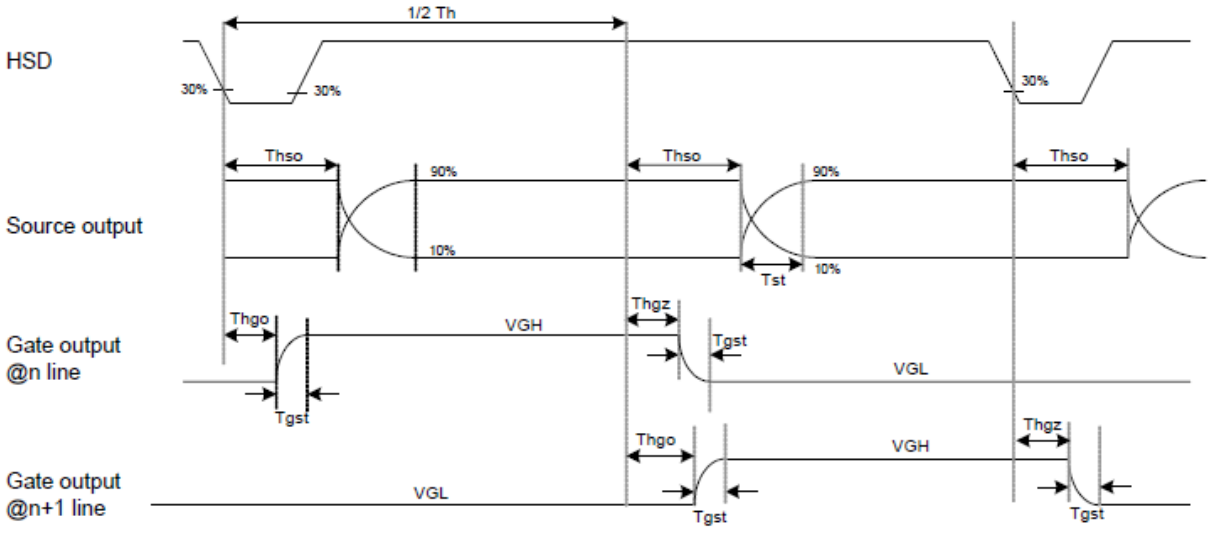
Note 8-7: Vertical sync signal, it is a “Low “active signal.

Note 8-8: Dot clock signal for RGB interface, timing for data loading defined at rising edge.

8.2. Timing characteristics

8.2.1. Input timing AC characteristics





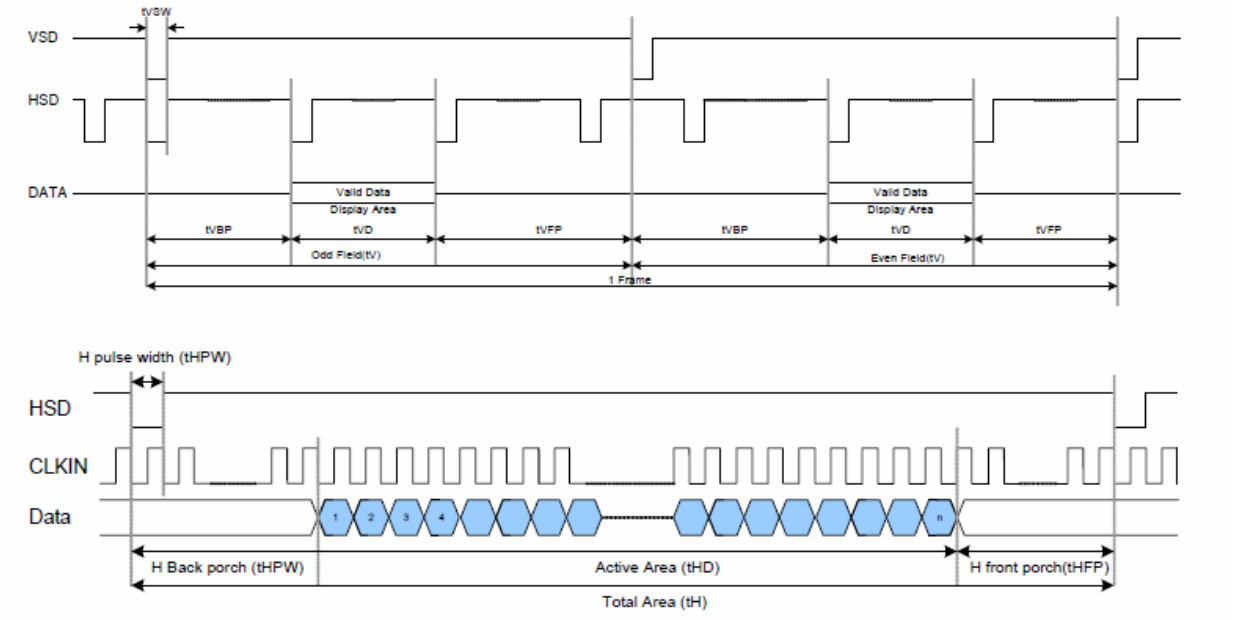
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Time that the HSD to CLKIN	Thc	-	-	1	CLKIN	
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	DR0~DR7, DG0~DG7, DB0~DB7 to CLKIN
Data hold time	Tdhd	12	-	-	ns	DR0~DR7, DG0~DG7, DB0~DB7 to CLKIN
Time that VSD to 1st Gate output	Tstv	0	21	31	H	@ 8-bit RGB, 8-bit Dummy RGB NTSC, and Parallel RGB, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	0	22	31	H	@ CCIR656 NTSC, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	3	24	34	H	@ 8-bit Dummy RGB & CCIR656 PAL, Delay by VBLK setting.
Source output setting time (*1)	Tst	-	-	8	us	R= TBD Kohm , C= TBD pF 10% 90%
Gate output setting time (*1)	Tstg	-	0.5	1	us	R= TBD Kohm , C= TBD pF 10% 90%
VCOM setting time (*1)	Tst,vcom	-	-	9	us	R= TBD Kohm , C= TBD nF 10% 90%
Time that HSD width	Twh	1	-	-	CLKIN	

PS,.(*1) Test Condition:

When the tested signal is change from V0,min to V0,max,the time that is from the start of change to the time that wing voltage at point B is less than +/-20 mV is called the setting time of the tested signal.

8.2.2. Input Timing format

8-bit RGB/8-bit Dummy RGB/YUV/Parallel RGB Input time chart



8-bit RGB input timing

Parameter		Symbol	Interface			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	13.5	27	27.19	MHz
HSD period		tH	1024	1716	1728	CLKIN
HSD display period		tHD		960		CLKIN
HSD back porch		tHBP	50	70	255	CLKIN
HSD front porch		tHFP	14	686	718	CLKIN
HSD pulse width		tHSW	1	1	tHBP-1	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	1	21	31	H
	Even field		1.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1CLKIN	1CLKIN	6H	
1 Frame			485	525	901	H

8-bit Dummy RGB input timing

8-bit Dummy RGB（320mode/NTSC/24.535Mhz）input timing

Parameter		Symbol	Interface			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.535	30	MHz
HSD period		tH	1306	1560	1907	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	40	241	255	CLKIN
HSD front porch		tHFP	0	39	372	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	1	21	31	H
	Even field		1.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

8-bit Dummy RGB (320mode/PAL/24.375Mhz) input timing

Parameter		Symbol	Interface			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.375	30	MHz
HSD period		tH	1306	1560	1920	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	385	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

8-bit Dummy RGB (360 mode/NTSC/27Mhz) Input Timing

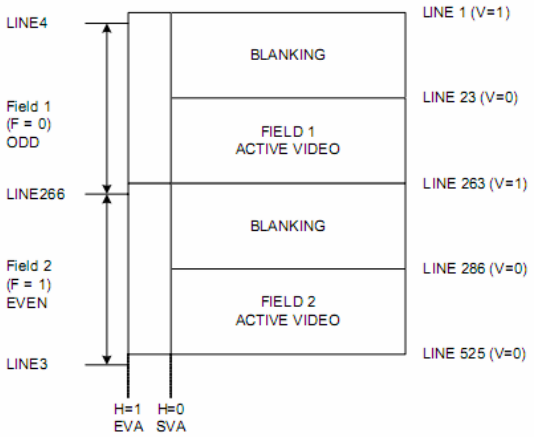
Parameter		Symbol	Interface			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1716	1907	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	35	212	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	1	21	31	H
	Even field		1.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

8-bit Dummy RGB (320 mode/PAL/24.375Mhz) Input Timing

Parameter		Symbol	Interface			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.375	30	MHz
HSD period		tH	1306	1560	1920	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	385	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

8.2.3. CCIR 656 vertical input timing

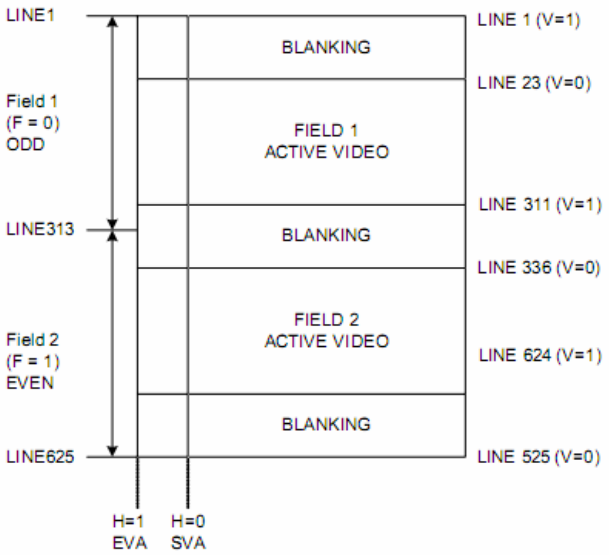
NTSC mode



LINE NUMBER	F	V	H (EVA)	H (SVA)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

PAL mode



LINE NUMBER	F	V	H (EVA)	H (SVA)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

8.2.4. YUV720 and YVU640 input timing

YUV720 mode/NTSC input timing

Parameter		Symbol	Min	Typ	Max.	Unit.
CLKIN Frequency		fCLKIN	--	27	--	MHz
HSD Period		tH	--	1716	--	CLKIN
HSD Display period		tHD		1440		CLKIN
HSD Back porch		tHBP	--	240	--	CLKIN
HSD Front porch		tHFP	--	36	--	CLKIN
HSD Pulse width		tHSW	--	1	--	CLKIN
VSD period time		tV	--	262.5	--	H
Vertical display area		tVD		240		H
VSD Back porch	Odd	tVBP	--	21	--	H
	Even		--	21.5	--	
VSD Front porch	Odd	tVFP	--	1.5	--	H
	Even		--	1	--	
VSD pulse width		tVSW	--	1	--	H
1 Frame			--	525	--	H

YUV720 mode/PAL input timing

Parameter		Symbol	Min	Typ	Max.	Unit.
CLKIN Frequency		fCLKIN	--	27	--	MHz
HSD Period		tH	--	1728	--	CLKIN
HSD Display period		tHD		1440		CLKIN
HSD Back porch		tHBP	--	240	--	CLKIN
HSD Front porch		tHFP	--	48	--	CLKIN
HSD Pulse width		tHSW	--	1	--	CLKIN
VSD period time		tV	--	312.5	--	H
Vertical display area		tVD		288		H
VSD Back porch	Odd	tVBP	--	24	--	H
	Even		--	24.5	--	
VSD Front porch	Odd	tVFP	--	0.5	--	H
	Even		--	0	--	
VSD pulse width		tVSW	--	1	--	H
1 Frame			--	625	--	H

YUV640 mode/NTSC input timing

Parameter		Symbol	Min	Typ	Max.	Unit.
CLKIN Frequency		fCLKIN	--	24.535	--	MHz
HSD Period		tH	--	1560	--	CLKIN
HSD Display period		tHD		1280		CLKIN
HSD Back porch		tHBP	--	240	--	CLKIN
HSD Front porch		tHFP	--	40	--	CLKIN
HSD Pulse width		tHSW	--	1	--	CLKIN
VSD period time		tV	--	262.5	--	H
Vertical display area		tVD		240		H
VSD Back porch	Odd	tVBP	--	21	--	H
	Even		--	21.5	--	
VSD Front porch	Odd	tVFP	--	1.5	--	H
	Even		--	1	--	
VSD pulse width		tVSW	--	1	--	H
1 Frame			--	525	--	H

YUV640 mode/PAL input timing

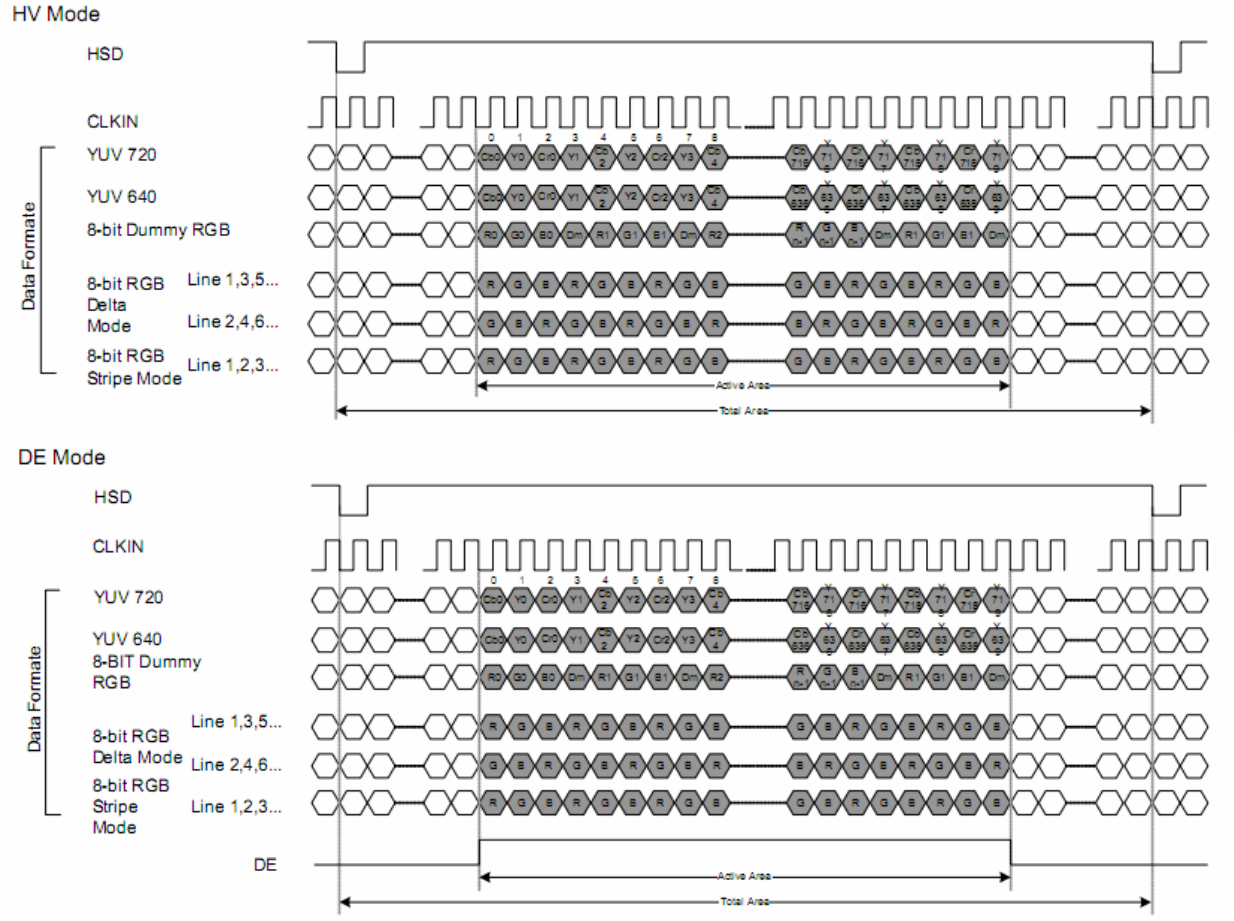
Parameter		Symbol	Min	Typ	Max.	Unit.
CLKIN Frequency		fCLKIN	--	24.375	--	MHz
HSD Period		tH	--	1560	--	CLKIN
HSD Display period		tHD		1280		CLKIN
HSD Back porch		tHBP	--	240	--	CLKIN
HSD Front porch		tHFP	--	40	--	CLKIN
HSD Pulse width		tHSW	--	1	--	CLKIN
VSD period time		tV	--	312.5	--	H
Vertical display area		tVD		288		H
VSD Back porch	Odd	tVBP	--	24	--	H
	Even		--	24.5	--	
VSD Front porch	Odd	tVFP	--	0.5	--	H
	Even		--	0	--	
VSD pulse width		tVSW	--	1	--	H
1 Frame			--	625	--	H

8.2.5. Parallel RGB Input Timing

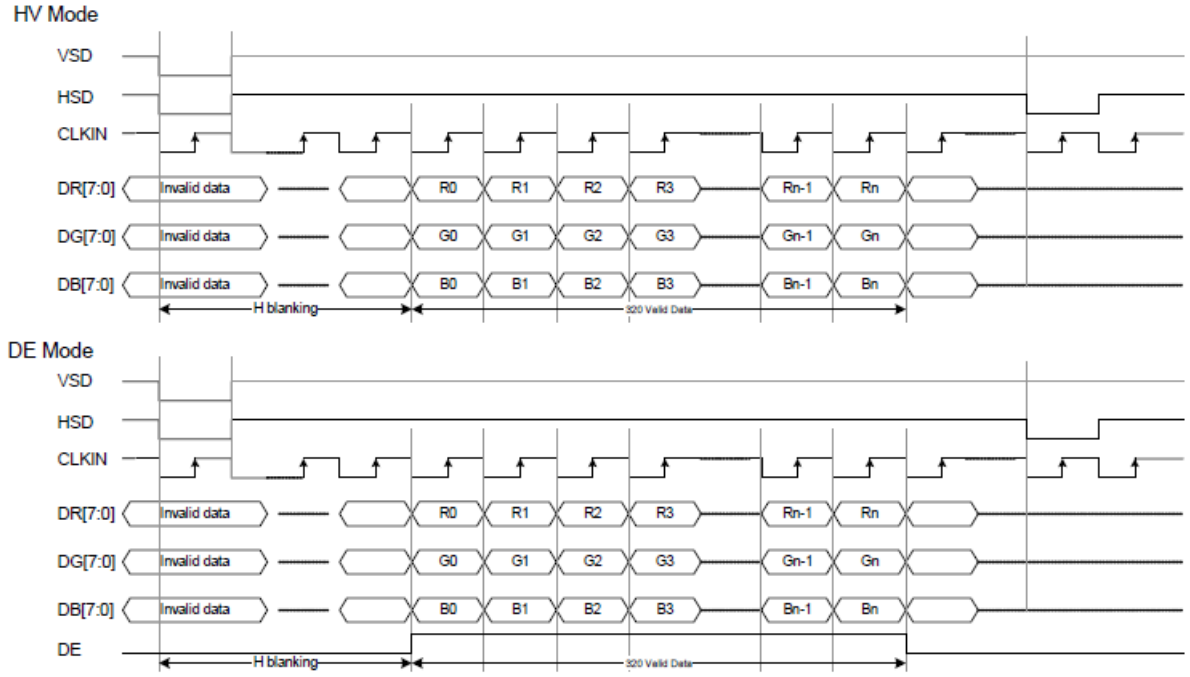
Parameter		Symbol	Min	Typ	Max.	Unit.
CLKIN Frequency		fCLKIN	--	6,2	7,5	MHz
HSD Period		tH	--	390	--	CLKIN
HSD Display period		tHD		320		CLKIN
HSD Back porch		tHBP	40	61	--	CLKIN
HSD Front porch		tHFP	--	9	--	CLKIN
HSD Pulse width		tHSW	--	1	--	CLKIN
VSD period time		tV	--	262.5	--	H
Vertical display area		tVD		240		H
VSD Back porch	Odd	tVBP	--	21	--	H
	Even		--	21.5	--	
VSD Front porch	Odd	tVFP	--	1.5	--	H
	Even		--	1	--	
VSD pulse width		tVSW	--	1	--	H
1 Frame			--	525	--	H

8.2.6. Data Input format

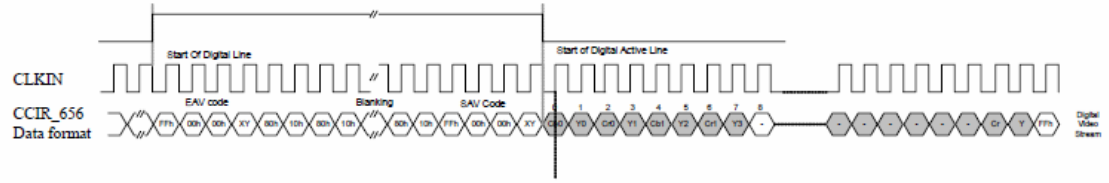
Serial 8-bit RGB/8-bit Dummy RGB/YUV Mode Data format



Parallel RGB Mode Data format



CCIR_656 MODE Data format



- FF 00 00 XY signals are involoved withHSD, VSD and Field.
- XY encode following bits:

  F = field select

  V = indicate vertical blanking

  H = 1, if EAV else 0 for SAV

  P3-P0 = protection bits:

  P3 = V⊕H P2=F⊕H P1=F⊕V P0=F⊕V⊕H ⊕:Represents the exclusive-OR function.

XY							
D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

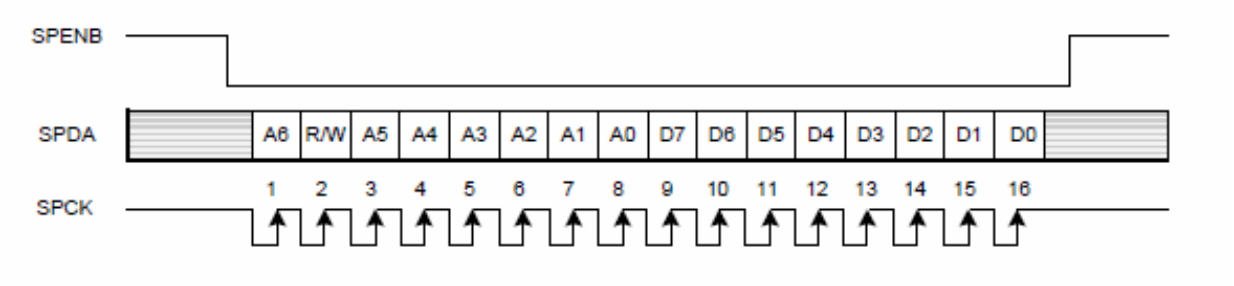
- Control is provided through "End of Video" (EAV) and "Start of Video" (SAV) timing references.
- Horizontal blanking section cosists of repeating pattern 80 10 80 10

8.2.7. Internal Register Description

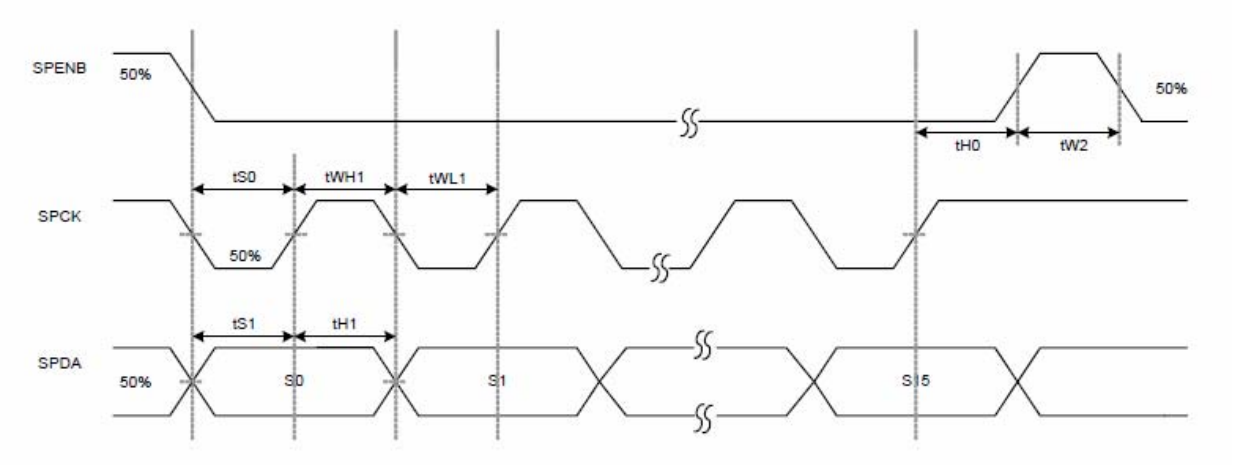
The 3-wire CPU serial interface is used and set to the data writing in these internal registers.

Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of serial clock SPCK. Command loading operation starts from the falling edge of SPENB and is completed at the next rising edge of SPENB

■ **3 Wire Serial command format**



■ **Serial Control timing**



Item	symbol	Min.	Typ.	Max.	Unit
SPENB input setup time	tS0	50			ns
Serial data input setup time	tS1	50			ns
SPENB input hold time	tH0	50			ns
Serial Data Input hold time	tH1	50			ns
SPCK pulse high width	tWH1	50			ns
SPCK pulse low width	tWL1	50			ns
SPENB pulse high width	tW2	400			ns

3-Wire Register table

Register	Address								Parameter Data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R00h	0	1/0	0	0	0	0	0	0	Y_CbCr (0)	CCIR601 (0)	x	x	VCOM_AC (0101)			
R01h	0	0	0	0	0	0	0	1	VCDCE (1)	x	VCOM_DC (21h)					
R03h	0	0	0	0	0	0	1	1	Brightness (40h)							
R04h	0	0	0	0	0	1	0	0	Narrow (0)	YUV (0)	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)
R05h	0	0	0	0	0	1	0	1	DRV_FREQ (0)	GRB (1)	PWM_DUTY (011)			SHDB2 (1)	SHDB1 (1)	STB (0)
R06h	0	0	0	0	0	1	1	0	HBLK_EN (0)	LED_Current (00)		VBLK (15h)				
R07h	0	0	0	0	0	1	1	1	HBLK (46h)							
R08h	0	1/0	0	0	1	0	0	0	BL_DRV (00)		x	x	x	0	0	0
R0Bh	0	1/0	0	0	1	0	1	1	REGSEL (0)		x	SYNCSEL	x	x	SOPC (11)	
R0Ch	0	1/0	0	0	1	1	0	0	PAIR (00)		DESEL (0)	CbCr (0)	Depol (0)	Vdpol (1)	Hdpol (1)	CLKINpol (0)
R0Dh	0	1/0	0	0	1	1	0	1	CONTRAST_B (40h)							
R0Eh	0	1/0	0	0	1	1	1	0	x	SUB_CONTRAST_R (40h)						
R0Fh	0	1/0	0	0	1	1	1	1	x	SUB_BRIGHTNESS_R (40h)						
R10h	0	1/0	0	1	0	0	0	0	x	SUB_CONTRAST_B (40h)						
R11h	0	1/0	0	1	0	0	0	1	x	SUB_BRIGHTNESS_B (40h)						
R12h	0	1/0	0	1	0	0	1	0	TRMEN (00)							
R13h	0	1/0	0	1	0	0	1	1	x	x	x	0	CF_SEL (0)	0	0	IN_SEL (0)
R16h	0	1/0	0	1	0	1	1	0	x	x	x	x	x	GAMMA2.2 (1)	x	x
R17h	0	1/0	0	1	0	1	0	1	x	GMA_V16 (101)			x	GMA_V8 (100)		
R18h	0	1/0	0	1	1	0	0	0	x	GMA_V50 (101)			x	GMA_V32 (100)		
R19h	0	1/0	0	1	1	0	0	1	x	GMA_V96 (100)			x	GMA_V72 (011)		
R1Ah	0	1/0	0	1	1	0	1	0	x	GMA_V120 (101)			x	GMA_V110 (100)		
R55h	1	1/0	0	0	0	1	0	1	0	INV_SEL (0)	0	0	x	X	X	0
R56h	1	1/0	0	0	0	1	1	0	x	x	x	x	x	x	VGH_SEL (11)	
R57h	1	1/0	0	0	0	1	1	1	x	x	x	x	x	x	VGL_SEL (10)	
R61h	1	1/0	0	1	0	1	1	1	x	x	x	x	x	x		FBMODE (1)

Note:

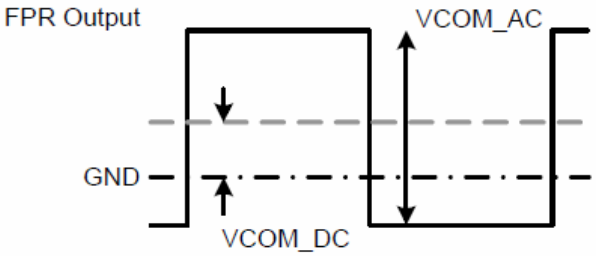
1. When RSTB is low, all registers reset to default values.
2. Serial commands are executed at next VSD signal.

■ R00h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R00h	Y_CbCr (0)	CCIR601 (0)	x	x	VCOM_AC (0101)			

VCOM_AC (R00h[3:0]): VCOM voltage AC level seletion

VCOM_AC[3:0]				Voltage(V)
0	0	0	0	3.6
0	0	0	1	3.7
0	0	1	0	3.8
0	0	1	1	3.9
0	1	0	0	4
0	1	0	1	**4.1(default)**
0	1	1	0	4.2
0	1	1	1	4.3
1	0	0	0	4.4
1	0	0	1	4.5
1	0	1	0	4.6
1	0	1	1	4.7
1	1	x	x	4.8



CCIR601 (R00h[6]): CCIR601 interface control

CCIR601	Function
0	Disable CCIR601. (**default**)
1	Enable CCIR601. (please refer to the table of R4(SEL) for detail descrption

Y_CbCr (R00h[7]): Y & CbCr exchange position (only valid for 8-bit input YUV640/YUV720)

	Under R12[4] CbCr = '0'							
Y_CbCr = '0' (**default**)	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3
Y_CbCr = '1'	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2

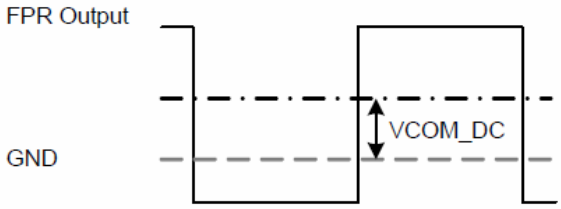
Under R12[4] CbCr = '1'							
Cr0	Y0	Cb0	Y1	Crb2	Y2	Cb2	Y3
Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

■ R01h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R01h	VCDCE (1)	x	VCOM_DC (21h)					

VCOM_DC (R01h[5:0]): VCOM voltage DC level selection (20mV/step)

VCOM_DC[5:0]	VCOM DC Level
00h	0.24
:	:
21h	0.90 (**default**)
:	:
3Fh	1.5



VCDCE (R01h[7]): VCOM DC enables control

VCDCE	VCDCE Fuction
0	VCOM DC function disabled. The VCOMDC pin is connected to GND.
1	VCOM DC function enabled. The VCOMDC voltage follows VCOM_DC setting. (**default**)

■ R03h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R03h	Brightness (40h)							

Brightness (R03h[7:0]): RGB brightness level control

Brightness[7:0]	Brightness Offset
00h	Dark. (-64)
40h	Center (0).(default)
FFh	Bright. (+191)

Setting accuracy 1bit/step

■ R04h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R04h	Narrow (0)	YUV (0)	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)

HDIR(R04h[0]): Source driver output direction selection

HDIR	HDIR Function
0	Shift from right to left. Y0 ←Y1←...←Y959←Y960
1	Shift from left to right. Y0→Y1→...→Y959→Y960(**default**)

VDIR(R04h[1]): Gate driver output direction selection

VDIR	VDIR Function
0	Shift from down to up. L0 ←L1←...←L959←L960
1	Shift from up to down. L0→L1→...→L959→L960(**default**)

NTSC/PAL[1:0] (R04h[3:2]): NTSC/PAL input mode selection.

NTSC/PAL[1:0]		NTSC/PAL Mode
0	0	PAL.
0	1	NTSC
1	X	Auto detection. (**default**)

SEL[1:0] (R04h[5:4]): Input data format selection.

CCIR601	YUV	SEL[1:0]		Input Timing format
0	0	0	0	8-bit RGB. (**default**)
0	0	0	1	8-bit Dummy RGB 320 x 240
0	0	1	x	8-bit Dummy RGB 360 x 240
0	1	0	x	CCIR656(720)
0	1	1	x	CCIR656(640)
1	1	0	x	YUV640
1	1	1	0	YUV720

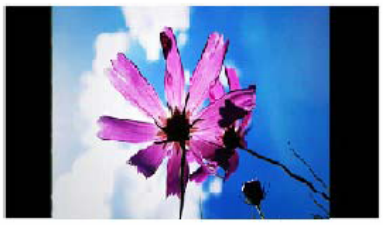
YUV(R04h[6]): YUV(CCIR656) or RGB input interface selection.

YUV	Data format
0	RGB input. (Default)
1	CCIR656/YUV640/YUV720 input

Narrow(R04h[7]): Normal / Narrow display selection

Narrow	Function
0	Normal display. (Default)
1	Narrow display.

Narrow = 0



Narrow = 1

■ R05h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R05h	DRV_FREQ (0)	GRB (1)	PWM_DUTY (011)			SHDB2 (1)	SHDB1 (1)	STB (0)

STB(R05h[0]): Standby (Power saving) mode control

STB	STB Function
0	Standby Mode. (default)
1	Normal operation.

SHDB1(R05h[1]): Back light power converter control.

SHDB1	SHDB1 Funciton
0	The back light power converter is off.
1	The back light power converter is controlled by STB's power on/off sequence. (default)

SHDB2(R05h[2]): VGH/VGL charge pump control

SHDB2	SHDB2 Funciton
0	VGH/VGL charge pump is always off.
1	VGH/VGL charge pump is controlled by STB's power on/off sequence. (default)

PWM_DUTY(R05h[5:3]): PWM duty cycle selection for back light power convert

PWM_DUTY[2:0]			PWM duty cycle
0	0	0	55%
0	0	1	60%
0	1	0	65%
0	1	1	70% (default)
1	0	0	75%
1	0	1	80%
1	1	0	85%
1	1	1	90%

GRB(R05h[6]): Global reset

GRB	GRB Function
0	Reset all registers to default value.
1	Normal operation. (Default)

DRV_FREQ(R05h[7]): DRV signal frequency selection

DRV_FREQ	DRV frequency
0	High Frequency (default)
1	Low Frequency

■ R06h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R06h	HBLK_EN (0)	LED_Current (00)		VBLK (15h)				

VBLK[4:0](R06h[4:0]): Vertical blanking setting for 8-bit RGB , 8-bit Dummy RGB & CCIR656

For 8-bit RGB, 8-bit Dummy RGB, YUV640, YUV720, CCIR656 **NTSC** mode, and Parallel RGB input mode.

VBLK[4:0]	VBLK Function	Unit
00h~03h	3.	H
04h	4.	
15h	21.(**default**)	
1Fh	31.	

For 8-bit Dummy RGB, YUV640, YUV720, CCIR656 **PAL** mode (Vertical Blanking + 3)

VBLK[4:0]	VBLK Function	Unit
00h	3.	H
04h	7.	
15h	24.(**default**)	
1Fh	34.	

LED_CURRENT[0:1] (R06h[5:6]): LED current adjustable for DC-DC feedback threshold voltage

LED_CURRENT[1:0]	Feedback Threshold Voltage
0	0.6 V. (**default**)
1	0.75V.
10	0.45V.
11	0.3V.

HBLK_EN (R06h[7]): Horizontal blanking function enable

■ R07h

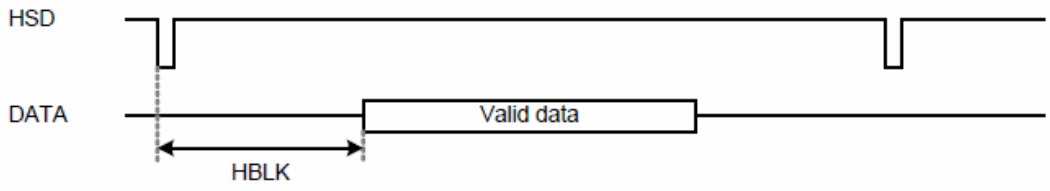
Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R07h	HBLK (46h)							

HBLK (R07h[7:0]): Horizontal blanking setting

HBLK_EN	D7~D0	HBLK	Unit	NTSC/PAL Mode
X	32h	50	CLKIN(*)	8-bit RGB
X	46h	70		
X	FFh	255		
X	X	241	CLKIN(*)	8-bit Dummy RGB
0	XXh	240	CLKIN(*)	YUV840, YUV720
1	00h~03h	3	CLKIN(*)	
	04h~255	4~255		
0	X	61	CLKIN(*)	Parallel RGB
	28h~	4~63		

*The frequency of CLKIN is different under different input timing.

'X' : don't care



■ R08h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R08h	BL_DRV (00)		x	x	x	0	0	0

BL_DRV(R08h[7:6]) : Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability. (Default)
0	1	2 times the Normal capability.
1	0	4 times the Normal capability.
1	1	8 times the Normal capability.

■ R0Bh

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Bh	REGSEL (0)		x	SYNCSEL	x	x	SOPC (11)	

SOPC (R0Bh[1:0]): Source output driving capability selection

D1	D0	Source Driver Capability
0	0	-50%.
0	1	-33%
1	0	-25%
1	1	Normal. (default)

SYNCSEL (R0Bh[4]): SYNC mode selection

D4	SYNCSEL Function
0	DE Mode
1	SYNC+DE Mode

REGSEL (R0Bh[7]): MTP function control register

D7	REGSEL Function
0	VCOM_DC[5:0] is read from MTP memory. (Default)
1	VCOM_DC[5:0] is controlled by the register R1.

■ R0Ch

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Ch	PAIR (00)		DESEL (0)	CbCr (0)	DEpol (0)	VDpol (1)	HDpol (1)	CLKINpol (0)

CLKINpol (R0Ch[0]): CLKIN polarity selection

D0	CLKINpol Function
0	Latch data at CLKIN rising edge. (Default)
1	Latch data at CLKIN falling edge

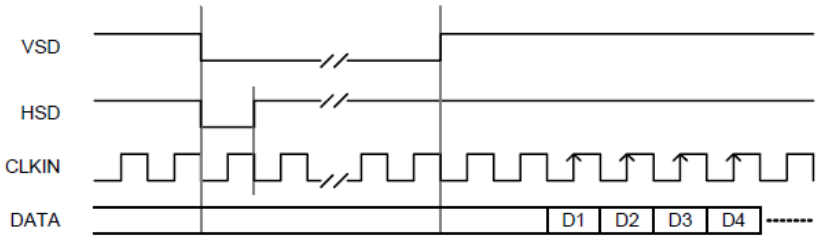
HDpol (R0Ch[1]): HSD polarity selection

D1	HDpol Function
0	Positive polarity.
1	Negative polarity. (Default)

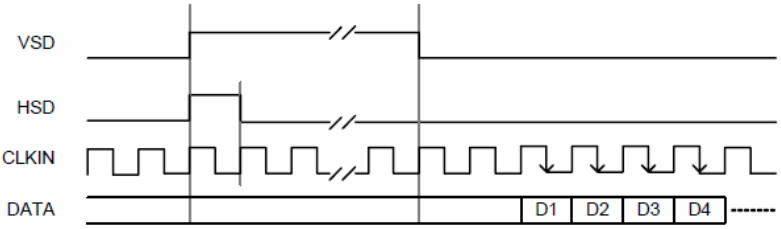
VDpol (R0Ch[2]): VSD polarity selection

D2	VDpol Function
0	Positive polarity.
1	Negative polarity. (Default)

HDpol = 1, VDpol = 1, CLKINpol = 0



HDpol = 0, VDpol = 0, CLKINpol = 1



DEpol (R0Ch[3]): DEN polarity selection

D3	DEpol Function
0	Positive polarity (Default)
1	Negative polarity

CbCr (R0Ch[4]): Cb & Cr exchange position (valid for CCIR656 and YUV640/YUV720)

D4	CbCr Function
0	Cb→Y→Cr. (Default)
1	Cr→Y→Cb.

DESEL(R0Ch[5]): DE mode selection

D5	DESEL Function
0	HV mode selected. (Default)
1	DE mode selected.

SYNCSEL	DESEL	Function
0	0	HV Mode
	1	DE Mode
1	X	SYNC + DE

* DESEL only controls the HV and DE mode at 8-bit RGB, 8-bit Dummy RGB and Parallel Mode.

PAIR(R0Ch[7:6]): Vertical start time of odd/even frame

8-bit RGB / 8-bit Dummy RGB NTSC / 8-bit Dummy RGB PAL(*)

Parallel RGB input mode (PSEL= "Low")

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
X	0	21/21. (Default)	H(Line)
X	1	21/20.	

CCIR656/YUV640/YUV720 NTSC/PAL(**)

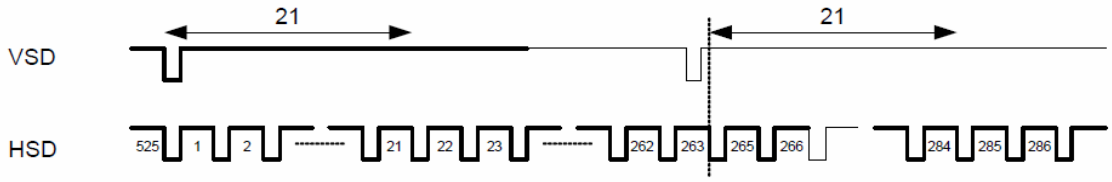
PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	21/21. (Default)	H(Line)
0	1	21/22	
1	0	22/21	
1	1	22/22	

(*)The typical value of VBLK of 8-bit Dummy RGB PAL (24 H) is different from 8-bit RGB/8-bit Dummy RGB NTSC(21H).

(**) The typical value of VBLK of CCIR656 PAL (24 H) is different from CCIR656 NTSC (21H).

Note: V-Blanking must be adjusted base on the input data.

For example:



■ R0Ch

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Ch	CONTRAST_B (40h)							

CONTRAST_B(R0Ch[7:0]) : RGB contrast level setting

D7~D0	Contrast Gain
00h	0
…	…
40h	1(Default)
…	…
FFh	3.984

■ R0Dh

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Dh	x	SUB_CONTRAST_R (40h)						

SUB-CONTRAST_R(R0Dh[6:0]): Red color contrast level setting

D6~D0	R Contrast Gain
00h	0.75
…	…
40h	1(Default)
…	…
7Fh	1.246

■ R0Eh

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Eh	x	SUB_BRIGHTNESS_R (40h)						

SUB-BRIGHTNESS_R(R0Eh[6:0]): Red color brightness level setting

D6~D0	R Brightness Offset
00h	darker (-64)
…	…
40h	center (0) (Default)
…	…
7Fh	brighter (+63)

■ R10h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R10h	x	SUB_CONTRAST_B (40h)						

SUB-CONTRAST_B(R10h[6:0]):Blue color contrast level setting

D6~D0	B Contrast Gain
00h	0.75
…	…
40h	1 (Default)
…	…
7Fh	1.246

■ R11h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R11h	x	SUB_BRIGHTNESS_B (40h)						

SUB-BRIGHTNESS_B(R11h[6:0]): Blue color brightness level setting

D6~D0	B Brightness Offset
00h	darker (-64)
…	…
40h	center (0) (Default)
…	…
7Fh	brighter (+63)

■ TRMEN(R12h):VCOM DC Trim Function Control Register

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R12h	TRMEN (00)							

TRMEN (R12h): VCOM DC Trim Function Control Register

VCOMDC Trim function control register, Write the follow command sequentially to enable the VCOMDC trim function.

Adjust VCDC level:

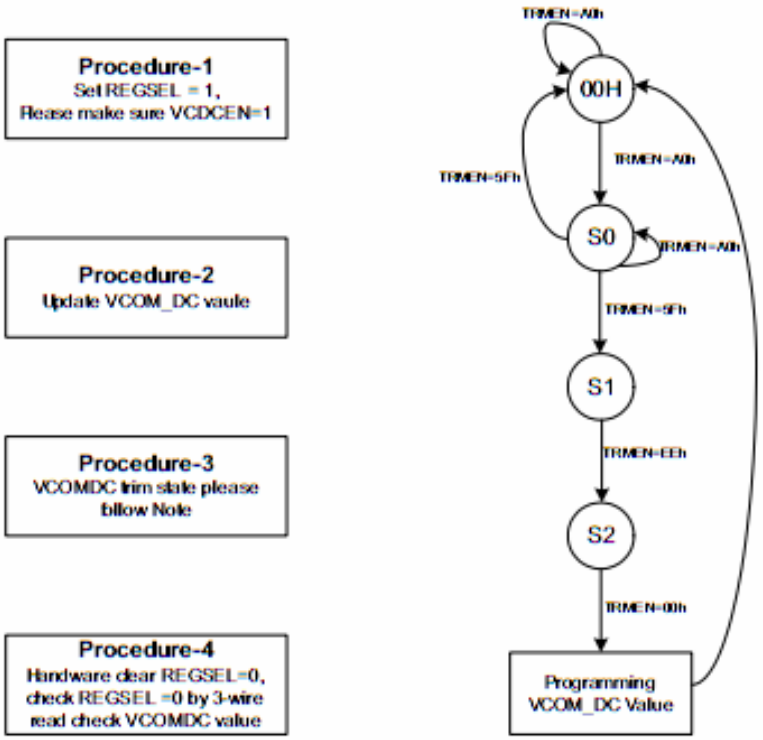
Set TRMEN[7:0] = 00h and write proper VCOM_DC[5:0] value using 3-wire command.

Programming the VCOM_DC value into MTP memory:

Set VPP_MTP = 7.5V with external power supply for programming operation. (Requirement)

Set TRMEN[7:0] as following sequence : A0h → 5Fh → EEh →00h

REGSEL will be clear to 0 after the programming procedure.



Note:

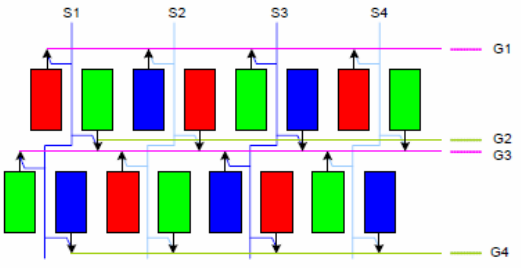
1. The Trim Block can be writing for only "4" times
2. After finishing TRMEN command do not power off within 1 second.
3. Trim command exceed the limition may cause the VCOMDC output unknown value.
4. The CLKIN input frequency should be 24MHz ~ 26MHz.

■ R13h

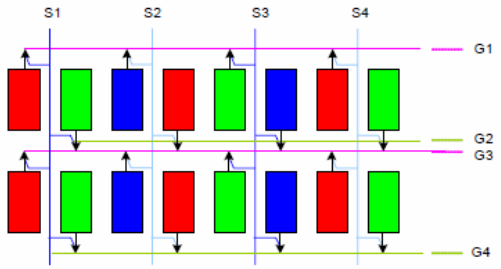
Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R13h	x	x	x	0	CF_SEL (0)	0	0	IN_SEL (0)

CF_SEL(R13h[3]): Color filter selection

CF_SEL	Function
0	Delta color filter. (Default)
1	Stripe color filter.



Delta Color Filter



Stripe Color Filter

IN_SEL(R13h[0]): Entry Control

IN_SEL	Function
0	Through mode: Input data must be aligned with the color filter arrangement.
1	Alignment mode: Input data must always be the R1, G1, B1,R2, G2, B2, … sequence, and the R/G/B data will be swapped automatically based on the selected color filter arrangement.

■ R16h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R16h	x	x	x	x	x	GAMMA2.2 (1)	x	x

GAMMA2.2 (R16h): Select auto or manual gamma setting

D2	Gamma 2.2 Function
0	Manual set gamma by R17h~R1Ah.
1	Auto set to gamma2.2. (default)

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R17h	x	GMA_V16 (101)			x	GMA_V8 (100)		
R18h	x	GMA_V50 (101)			x	GMA_V32 (100)		
R19h	x	GMA_V96 (100)			x	GMA_V72 (011)		
R1Ah	x	GMA_V120 (101)			x	GMA_V110 (100)		

Registers : R17h ~R1Ah

GMA_V8: Gamma reference voltage V8;

GMA_V16: Gamma reference voltage V16;

GMA_V32: Gamma reference voltage V32;

GMA_V50: Gamma reference voltage V50;

GMA_V72: Gamma reference voltage V72;

GMA_V96: Gamma reference voltage V96;

GMA_V110: Gamma reference voltage V110;

GMA_V120: Gamma reference voltage V120;

■ R55h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R55h	0	INV_SEL (0)	0	0	x	X	X	0

INV_SEL (R55h[6]): Inversion selection

D6	INV_SEL Function
0	One line inversion. (Default)
1	Column inversion.

■ R56h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R56h	x	x	x	x	x	x	VGH_SEL (11)	

VGH_SEL (R56h[1:0]): VGH voltage level selection

	VGH Voltage	
VGH_SEL	FBMODE=1	FBMODE=0
2'b00	|VGL| + 9V.	|VGL| + 2V.
2'b01	|VGL| + 10V.	|VGL| + 3V.
2'b10	|VGL| + 11V.	|VGL| + 4V.
2'b11	|VGL| + 12V. (Default)	|VGL| + 5V. (Default)

■ R57h

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R57h	x	x	x	x	x	x	VGL_SEL (10)	

VGL_SEL (R57h[1:0]): VGL voltage level selection

	VGH Voltage	
VGH_SEL	FBMODE=1	FBMODE=0
2'b00	-4V	-8V
2'b01	-5V	-9V
2'b10	-6V (default)	-10V (default)
2'b11	-7V	-11V

■ R61h

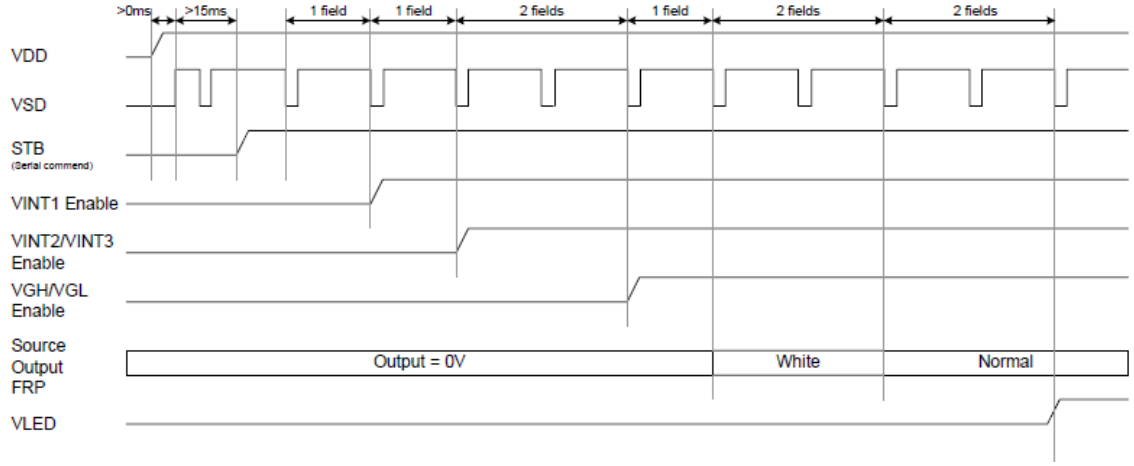
Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R61h	x	x	x	x	x	x		FBMODE

FBMODE	VGH/VGL Voltage Range selection
0	Select higher VGL voltage
1	Select lower VGL voltage

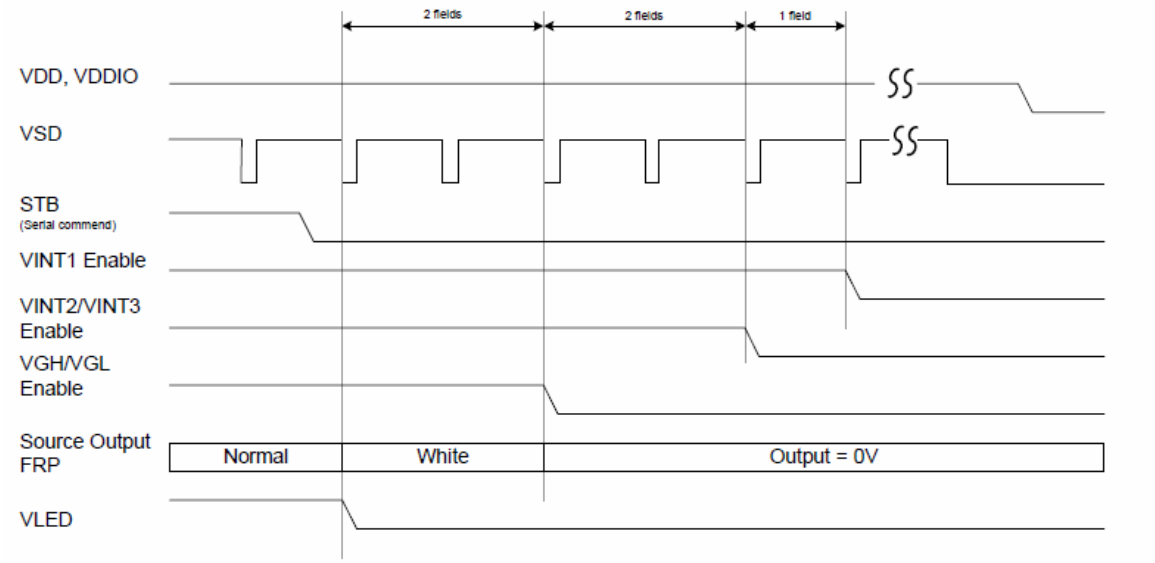
9. POWER ON/OFF SEQUENCE

Special care should be taken that the large current may cause a permanent damage to the LSI when voltage is applied to the LCD drive power supply terminals in the condition that the logic power supply terminals are floating.

9.1. Power ON Sequence



9.2. Power Supply OFF Sequence

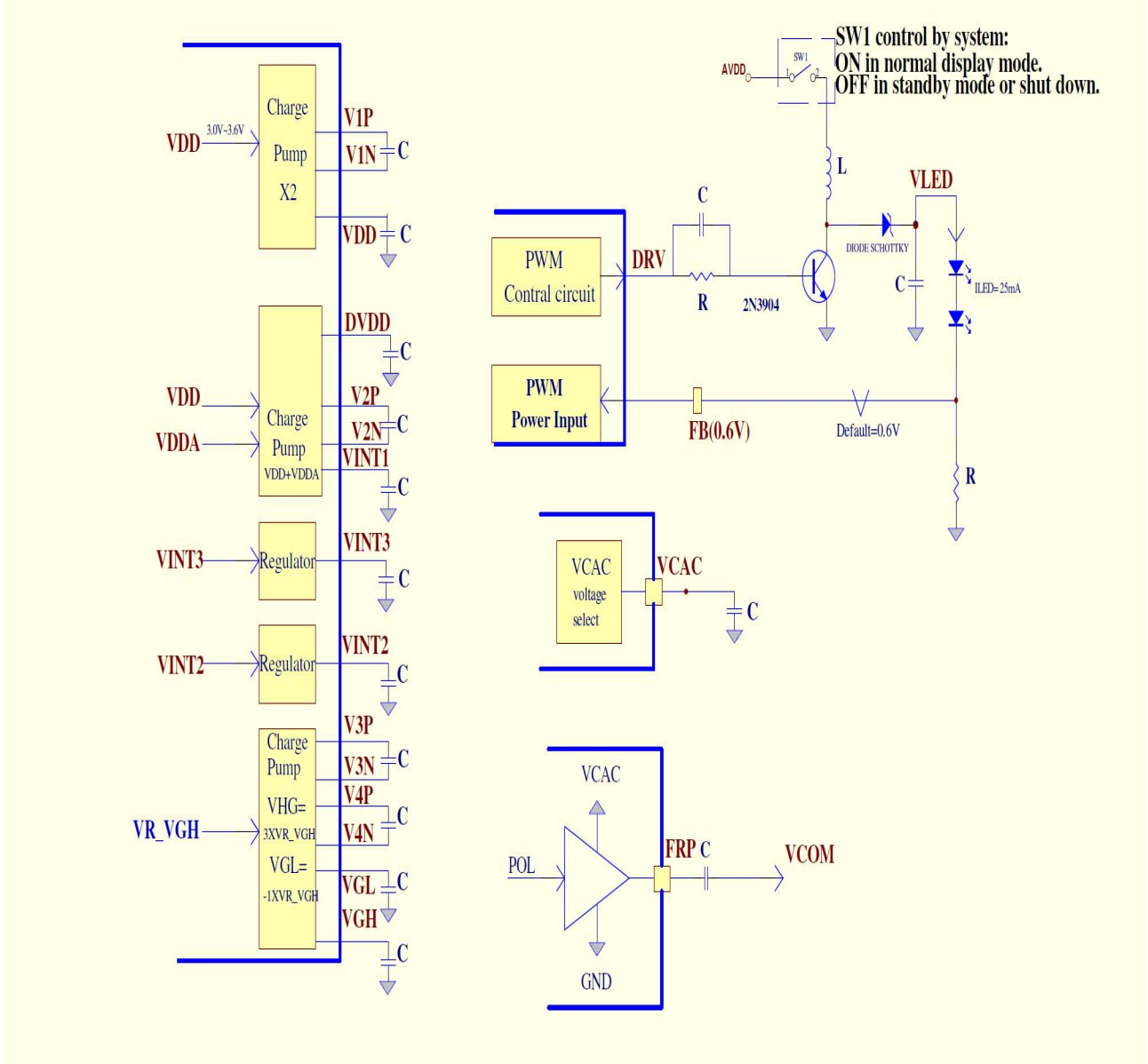


10. BLOCK DIAGRAM OF LCM

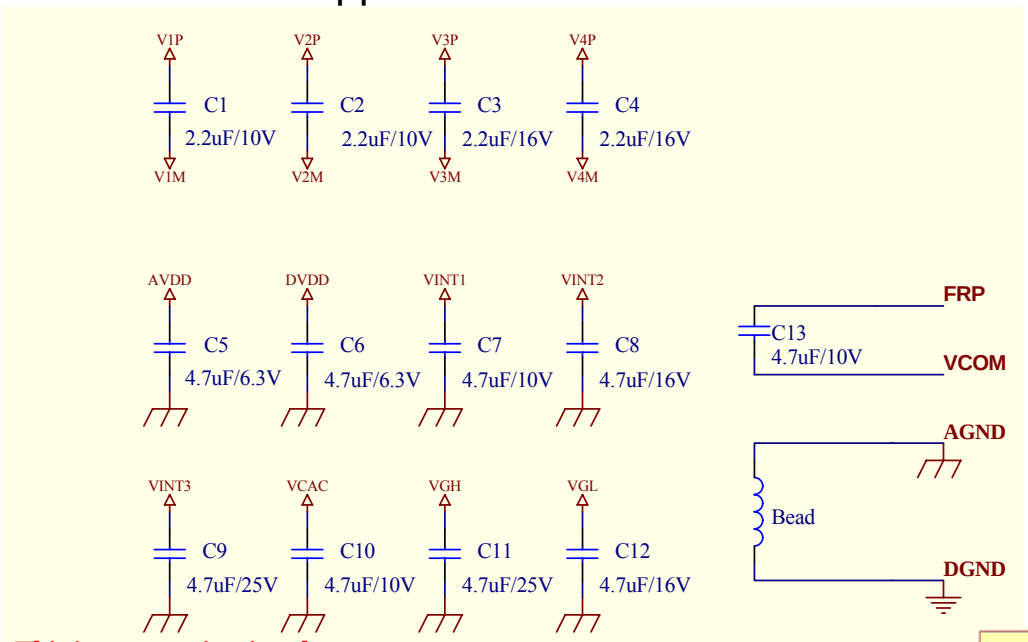
10.1. Display Color and Gray Scale Reference

Color		Input Color Data																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

10.2. Reference Circuit for LCD Module



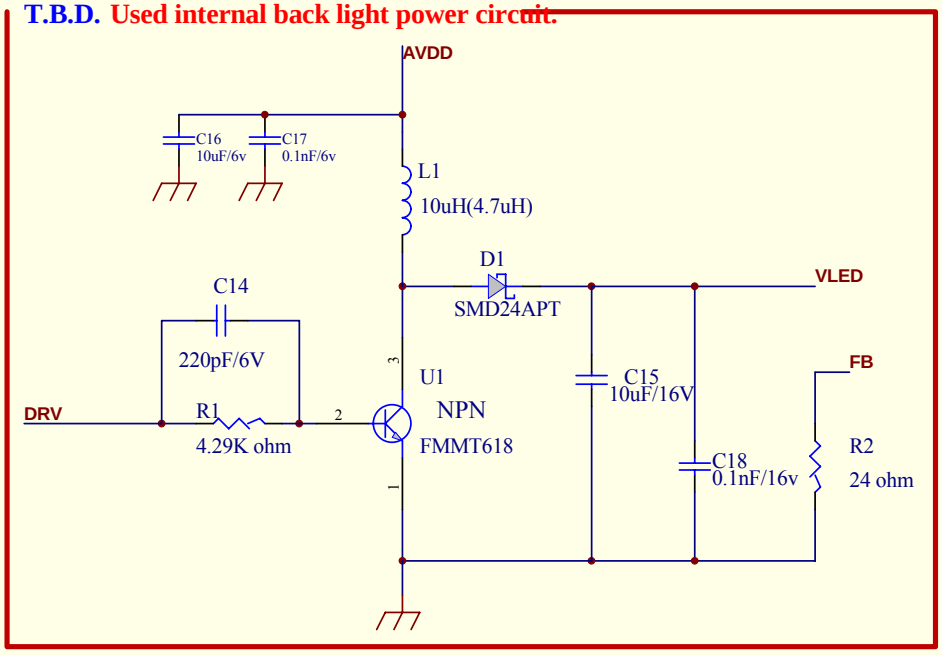
10.3. Reference Application Note

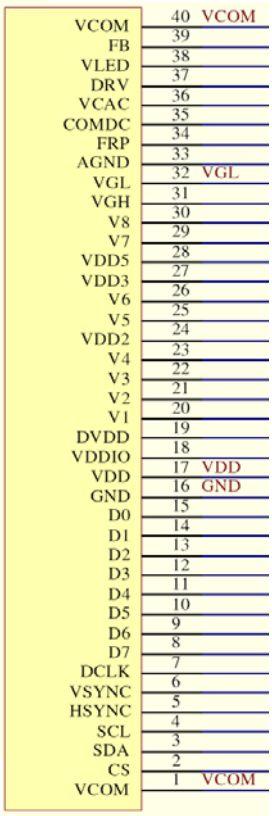


This is suggest circuit only

The device characteristic should by selected component

T.B.D. Used internal back light power circuit.

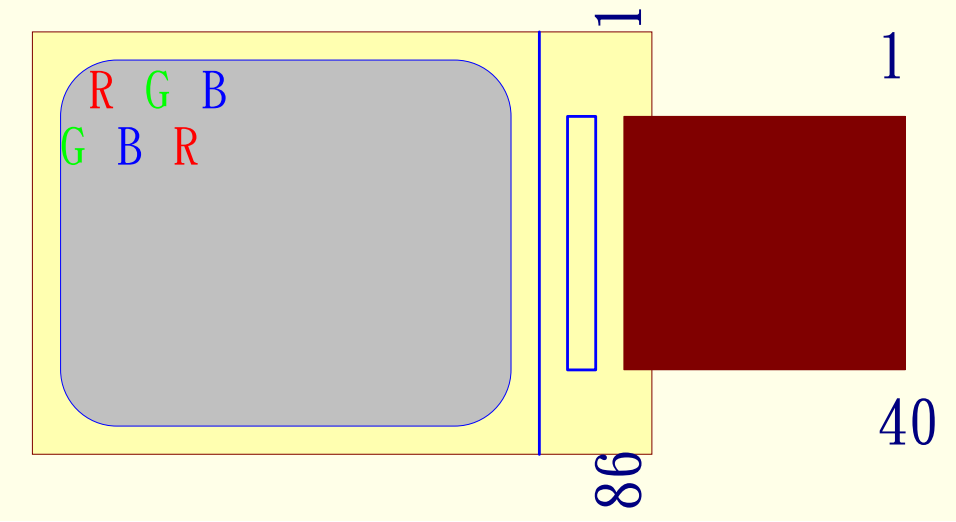




Remark:

When customers would like to use the internal backlight driver IC application circuit, customers would be recommended to follow the design rule above.

10.4. Pixel arrangement and input pin connector No.



11. ELECTRO-OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in dark room or equivalent state with the methods shown in Note 1,Note2,Note3.

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
Response time		T_R	Θ=0	-	20	30	ms	Note 4,6
		T_F		-	10	15	ms	
Contrast ratio		CR	At optimized viewing angle	-	300	-	-	Note 5,6
Viewing Angle	Hor.	$Θ_R$	CR≧ 10	35	45	-	Degree	Note 6,7
		$Θ_L$		50	60	-		
	Ver.	$φ_H$		50	60	-		
		$φ_L$		50	60	-		
White Chromaticity shift		X	Θ=0	0.30	0.34	0.38	-	
		Y		0.31	0.35	0.39		
Brightness			Θ=0	200	250	-	-	

Note1:Ambient temperature=25℃

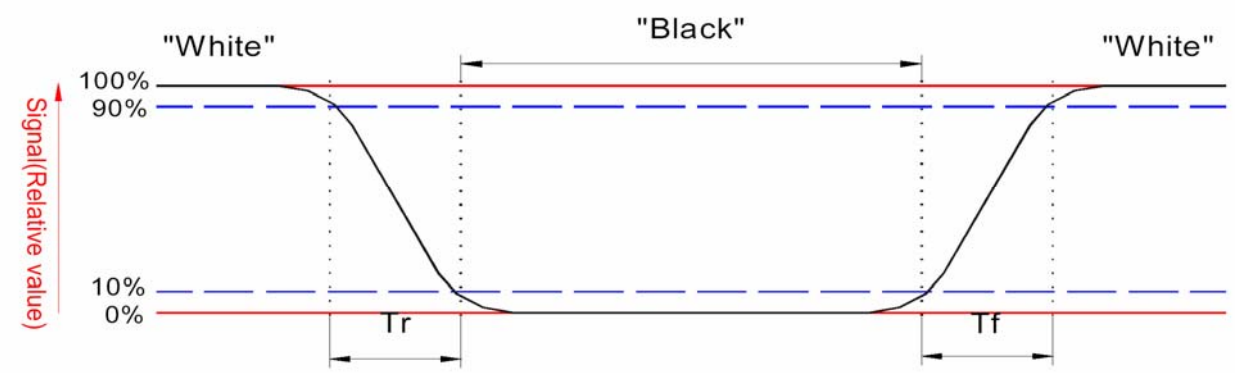
Note2:To be measured in the dark room.

Note3:To be measured on the center area of panel with a field angle of 1℃ by Topcon luminance meter BM-7,after 10 minutes operation.

Note4:Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black”to”white”(falling time) and from “white”to”black” (rising time),respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



Note5: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness measured when LCD is at “white state”}}{\text{Brightness measured when LCD is at “black state”}}$$

Note6:White Vi=V_{i50} $\overline{+}$1.5V

Black Vi=V_{i50} ± 2.0V

“±”means that the analog input signal swings in phase with COM signal.

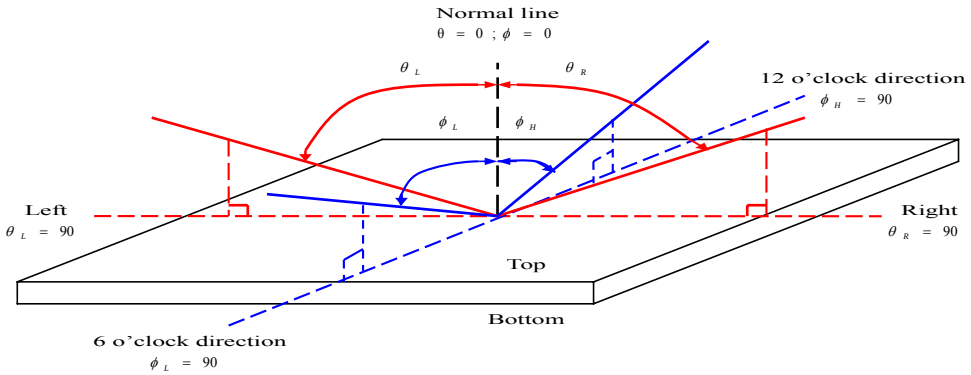
“+”means that the analog input signal swings out of phase with COM signal.

V_{i50} :The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all The input terminals of module are electrically opened.

Note7:Definition of viewing angle:

Refer to figure as below.



12. RELIABILITY

12.1. MTTF

The LCD module shall be designed to meet a minimum MTTF value of 50,000 hours with normal condition. (25°C in the room without sunlight; not include lifetime of backlight and Touch Panel).

12.2. Tests

NO.	ITEM	CONDITION	CRITERION
1	High Temperature Operating	70℃ 240 hrs	◦ No defect of Operational function in room temperature are allowable. ◦ Leakage current should be below double of initial value.
2	Low Temperature Operating	-20℃ 240 hrs	
3	High Temperature Non-Operating	80℃ 240 hrs	
4	Low Temperature Non-Operating	-30℃ 240 hrs	
5	High Temperature/ Humidity Non-Operating	50℃ , 90%RH 240 hrs	
6	Temperature Shock Non-Operating	-30℃ ⟷ 80℃ (30min) (5min) (30min) 10 CYCLES	
7	Electro-static Discharge	HBM: ±2kv	

Note 1: Test after 24 hours in room temperature(23±5°C).
Note 2: The sampling above is individually for each reliability testing condition.
Note 3: The color fading of polarizing filter should not care.
Note 4: All of the reliability testing chamber above, is using D.I. water.(Min value:1.0 MΩ -cm)
Note 5: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

12.3. Color Performance

No.	ITEM	Criterion (initial)
1	Luminance	>50%
2	NTSC	>70%
3	Contrast Ratio	>50%

13. INSPECTION CRITERIA

13.1. Inspection Conditions

13.1.1. Environmental conditions

The environmental conditions for inspection shall be as follows

Room temperature: 23±5°C

Humidity: 50±20%RH

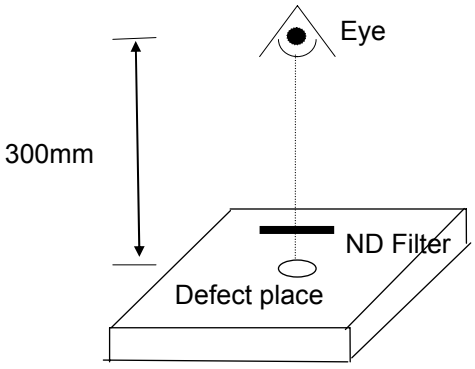
13.1.2 . The external visual inspection

With a single 1000±200lux fluorescent lamp as the light source, the inspection was in the distance of 30cm or more from the LCD to the inspector's eyes.

13.2. Light Method

13.2.1. Environment lamp under 1000 ± 200 lux, Viewing direction for inspectionover 30 ㎝

13.2.2. The distance from eye to defect around 300mm, the distance from NDFilter to defect around 25~30mm



13.3. Classification Of Defects

13.3.1. Major defect

A major defect refers to a defect that may substantially degrade usability

for product applications.

13.3.2. Minor defect

A minor defect refers to a defect which is not considered to be able substantially degrade the product application or a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation.

Notes: If the LCD/LCM ’s cosmetic and display performance do not specify in “inspection criterion”, it should be based on these delivered samples.

13.4. Sampling & Acceptable Quality Level

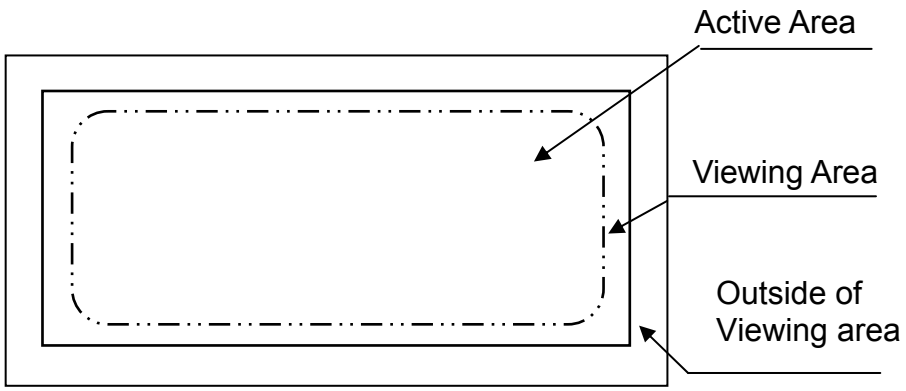
Level II, MIL-STD-105E

Inspection Item	Major defect	Minor defect
Cosmetic	1.0%	1.5%
Electrical test	0.4%	0.65%

13.5. Definition Of Inspection Area

V.A: Viewing Area

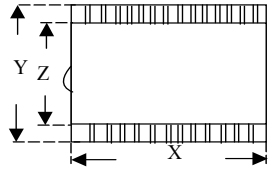
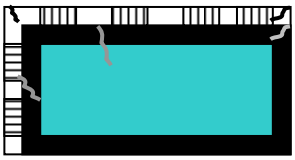
A.A: Active Area



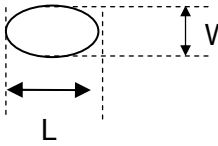
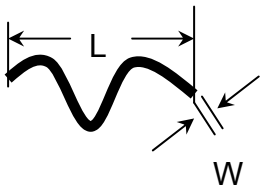
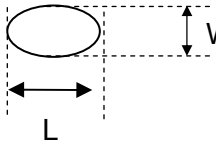
13.6. Items and Criteria

13.6.1. Visual inspection criterion in cosmetic

(1) Glass defect

Glass defect			
No	Defect	Criteria	Remark
1	Dimension (Minor)	By engineering diagram	
2	Cracks (Major)	Extensive crack 【Reject】	

(2) LCM appearance defect

No	Defect	Criteria		Remark
1	Round type (Minor)	Spec.	Permissible Qty	1. ϕ =(L+W)/2, L: Length, W: Width 2. Disregard if out of A.A. 3. Dots Distance ≧5mm 
		ϕ ≦0.10mm	Disregard	
		0.10mm< ϕ ≦ 0.20mm	3	
		0.20mm< ϕ	0	
2	Line type (Minor)	Spec.	Permissible Qty	1. L: Length, W: Width 2. Disregard if out of A.A. 
		W≦0.03mm	Disregard	
		L≦3.0mm and 0.03mm<W≦0.05mm	2	
		L≦3.0mm and 0.05mm<W≦0.10mm	1	
		W>0.10mm or L>3.0mm	0	
3	Polarizer dent (Minor)	Spec.	Permissible Qty	1. ϕ =(L+W)/2 , L: Length, W: Width 2. Disregard if out of A.A. 3. Dots Distance ≧5mm 
		ϕ ≦0.20mm	Disregard	
		0.20mm< ϕ ≦ 0.30mm	2	
		0.30mm< ϕ ≦ 0.50mm	1	
		0.50mm< ϕ	0	

(3) FPC

No	Defect	Criteria	Remark
1	Copper peeling (Minor)	Copper peeling 【Reject】	

(4) Black tape

No	Defect	Criteria	Remark
1	Shift (Minor)	IC exposed 【Reject】	
2	No black tape (Minor)	No black tape 【Reject】	

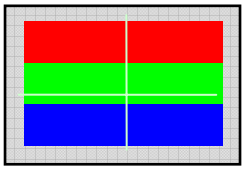
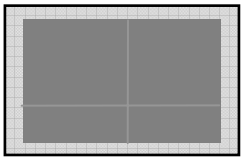
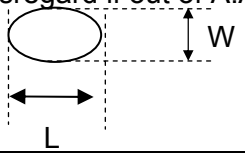
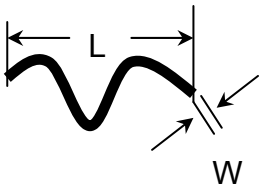
(5) Silicon

No	Defect	Criteria	Remark
1	Amount of silicon (Minor)	ITO exposed 【Reject】	

(6) Bezel

No	Defect	Criteria	Remark
1	Oxidized spot (Minor)	Oxidized spot, rust 【Reject】	
2	Outline deformation (Minor)	By engineering diagram	
3	Greasiness (Minor)	Greasiness 【Reject】	
4	Spots, round Type (Minor)	H≦By engineering diagram 【Disregard】	H=Total height (thickness)
5	Plating (Minor)	Bubble, peeling 【Reject】	

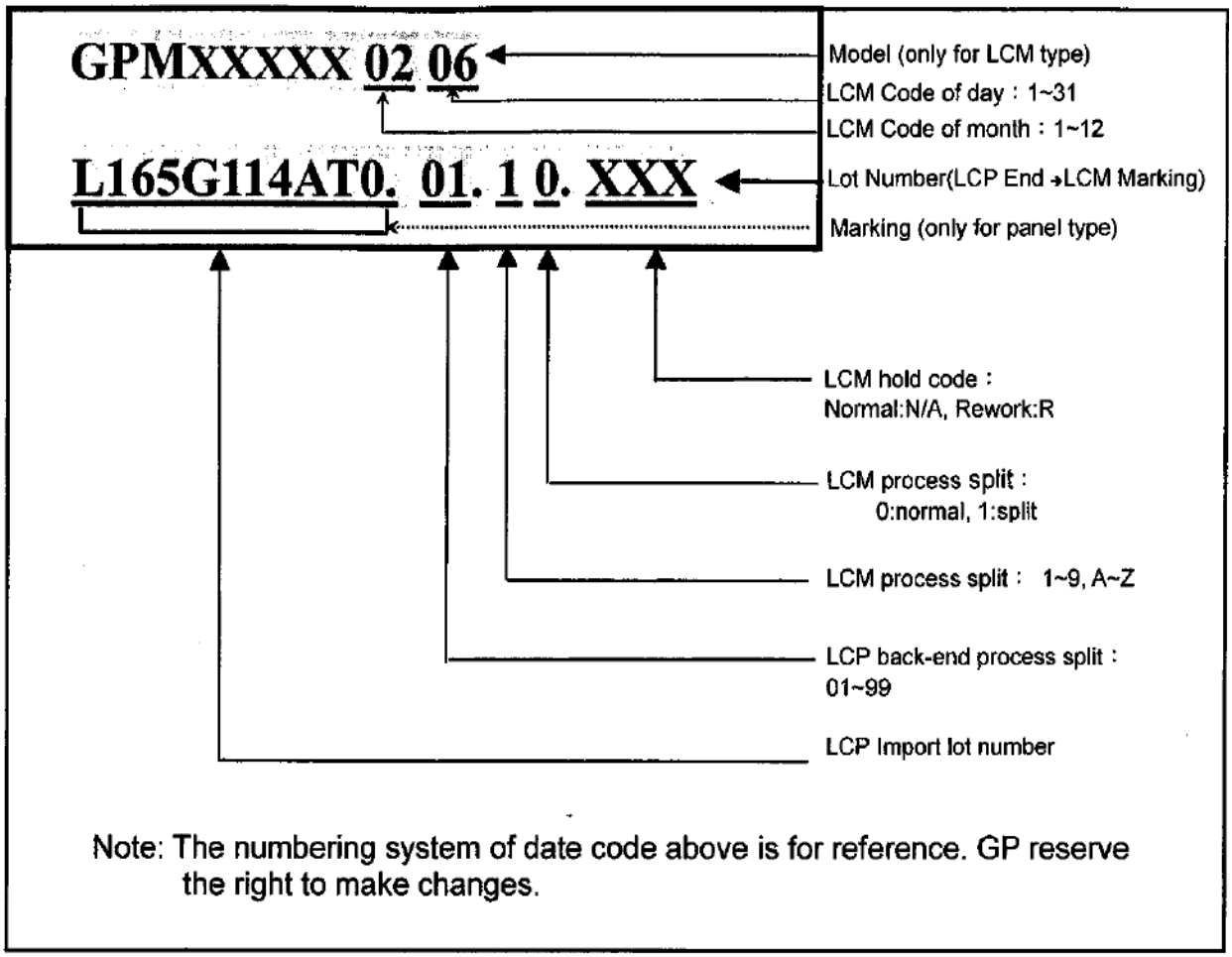
13.6.2. Visual inspection criterion in electrical display

No	Defect	Criteria		Remark
1	No display (Major)	Not allowed		
2	Missing line (Major)	Not allowed		
3	Darker or lighter line (Major)	Not allowed		
4	Weak line (Minor)	By limited sample		
5	Bright / Dark point (Minor)	Spec.	Permissible Qty	1:1sub-pixel: 1R or 1G or 1B 2:Point defect area≧ 1/2 sub pixel.
		Bright point	1	
		Dark point	2	
6	Round type (Minor)	Spec.	Permissible Qty	1. ϕ =(L+W)/2, L: Length, W: Width 2. Disregard if out of A.A. 
		$\phi \leqq$0.10mm	Disregard	
		0.10mm< $\phi \leqq$ 0.20mm	3	
		0.20mm< ϕ	0	
7	Line type (Minor)	Spec.	Permissible Qty	1. L: Length, W: Width 2. Disregard if out of A.A. 
		W≦0.03mm	Disregard	
		L≦3.0mm and 0.03mm<W≦0.05mm	2	
		L≦3.0mm and 0.05mm<W≦0.10mm	1	
		W>0.10mm or L>3.0mm	0	
8	Mura (Minor)	By 5% ND filter invisible		

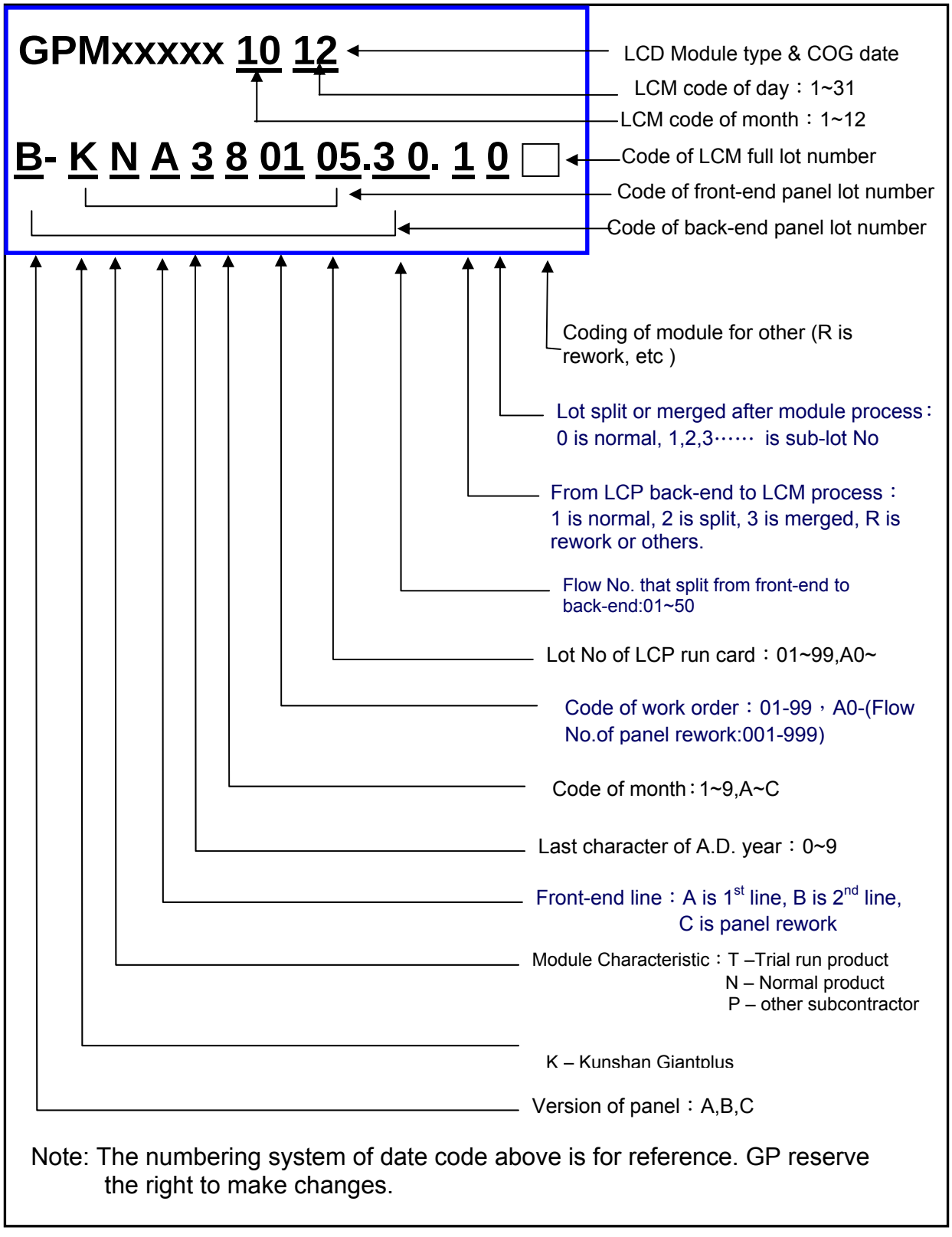
13.6.3. Others

1. Issues that are not defined in this document shall be discussed and agreed with both parties. (Customer and supplier)
2. Unless otherwise agreed upon in writing, the criteria shall be applied to both parties. (Customer and supplier)

14. ILLUSTRATION OF LCD DATE CODE(GP)



15. ILLUSTRATION OF LCD DATE CODE(KGP)



Note: The numbering system of date code above is for reference. GP reserve the right to make changes.

16. RoHS COMPLIANT WARRANTY

RoHs Hazardous substances including:

- Cd< 100 ppm
- Pb< 1000 ppm
- Hg< 1000 ppm
- Cr +6 < 1000 ppm
- PBDE < 1000 ppm
- PBB < 1000 ppm

17. PRECAUTIONS FOR USE

17.1. Safety

(1) Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.

(2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.

(3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

17.2. Storage Conditions

(1) Store the panel or module in a dark place where the temperature is 23±5°C and the humidity is below 50±20%RH.

(2) Store in anti-static electricity container.

(3) Store in clean environment, free from dust, active gas, and solvent.

(4) Do not place the module near organics solvents or corrosive gases.

(5) Do not crush, shake, or jolt the module.

(6) Do not exposed to direct sun light of fluorescent lamps.

17.3. Installing LCD Module

Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate or touch panel to protect the polarizer and LC cell.

(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm.

17.4. Precautions For Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (Vo). Adjust Vo to show the best contrast.
(2) Driving the LCD in the voltage above the limit will shorten its lifetime.
(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.
(4) When turning the power on, input each signal after the positive/negative voltage becomes stable.
(5) Do not apply water or any liquid on product which composed of T/P.

17.5. Handling Precautions

(1) Avoid static electricity which can damage the CMOS LSI; please wear the wrist strap when handling.
(2) The polarizing plate of the display is very fragile. so, please handle it very carefully.
(3) Do not give external shock.
(4) Do not apply excessive force on the surface; it may cause display abnormal .
(5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
(6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.
(7) Do not operate it above the absolute maximum rating.
(8) Do not remove the panel or frame from the module.
(9) Do not apply water or any liquid on product, which composed of T/P.

17.6. Warranty

(1) The period is within 12 months since the date of shipping out under normal using and storage conditions.
(2) The warranty will be avoided in case of defect induced by customer.

18. FACTORY

For the consideration of mass production convenience, this model will be manufactured in the factories listed below.

FACTORY NAME: GIANTPLUS TECHNOLOGY CO., LTD
FACTORY ADDRESS: 15 Industrial Rd., Lu-Chu Li, Toufen Town
351 Miao-Li County, Taiwan, R.O.C..
FACTORY PHONE: TEL: 886-37-611-611 FAX: 886-37-613-166
FACTORY ADDRESS: No.1127,Heping Rd.,Bade City,Taoyuan,334, Taiwan, R.O.C..
FACTORY PHONE: TEL: 886-3-3679978 FAX: 886-3-3670661

FACTORY NAME: KUNSHAN GIANTPLUS OPTOELECTRONICS
TECHNOLOGY CO., LTD.
FACTORY ADDRESS: KunShan City, JiangShu Province, China.
FACTORY PHONE: TEL:86-512-57780-988 FAX : 86-512-57780-503

FACTORY NAME: SHENZHEN GIANTPLUS OPTOELEC. DISPLAY CO., LTD.
FACTORY ADDRESS: Building A, Distict A ,MinZhu99 Industrial City,
ShaJing Industrial Park, BaoAn District, ShenZhen, China
FACTORY PHONE: TEL: 86-755-29720-088 FAX : 86-755-29720-828

19. REVISION HISTORY

Version	Revise record	Date
A	New version	2009/02/18