*HIGH-VOLTAGE MIXED-SIGNAL IC*

# UC1602s

65COM x 102SEG Matrix LCD Controller-Driver

**Preliminary Specifications**
**Revision 0.1**

**January 27, 2006**

ULTRACHIP

*The Coolest LCD Driver, Ever!!*

# Table of Content

# UC1602s

*Single-Chip, Ultra-Low Power*
*65COM x 102SEG Matrix*
*Passive LCD Controller-Driver*

## INTRODUCTION

UC1602s is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power COM and SEG drivers, UC1602s contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation, and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

## MAIN APPLICATIONS

- Cellular Phones, and other battery operated palm top devices or portable Instruments

## FEATURE HIGHLIGHTS

- Single chip controller-driver for 65x102 graphics STN LCD panels.
- Support both row-ordered and column-ordered display buffer RAM access.
- Support industry standard 2-wire, 3-wire, 3/4-wire, and 4-wire serial bus ($I^2C$, S9, S8uc, S8).
- Ultra-low power consumption under all display patterns.
- Software programmable frame rates at 80 and 100 Hz.
- Self-configuring 7-x charge pump with on-chip pumping capacitors. Only 3 external capacitors to operate.
- On-chip bypass capacitor for $V_{LCD}$ makes $V_{LCD}$ bypass capacitor optional.
- On-chip Power-ON Reset and Software RESET commands, make RST pin optional.
- Very low pin count (9~10-pin) allows exceptional image quality in COG format on conventional ITO glass.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- $V_{DD}$ (digital) range: 1.8V ~ 3.3V
  $V_{DD}$ (analog) range: 2.6V ~ 3.3V
  LCD $V_{OP}$ range: 4.8V ~ 11.5V
- Software programmable 4 temperature compensation coefficients.
- Available in gold bump dies
  Bump pitch (COM and SEG) : 44 µM min.
  Bump gap : 15 µM min.
  Bump surface : 2204 $\mu M^2$

## ORDERING INFORMATION

| Part Number | MTP | $I^2C$ | Description |
|---|---|---|---|
| UC1602sGAA | No | Yes | Gold Bumped Die |



### General Notes

#### APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

#### USE OF $I^2C$

The implementation of $I^2C$ is already included and tested in all silicon. However, unless $I^2C$ licensing obligation is executed satisfactorily, it is not legal to use UltraChip product for $I^2C$ applications. Unless $I^2C$ version is ordered from UltraChip, the customer will take the responsibility for all such licensing liabilities.

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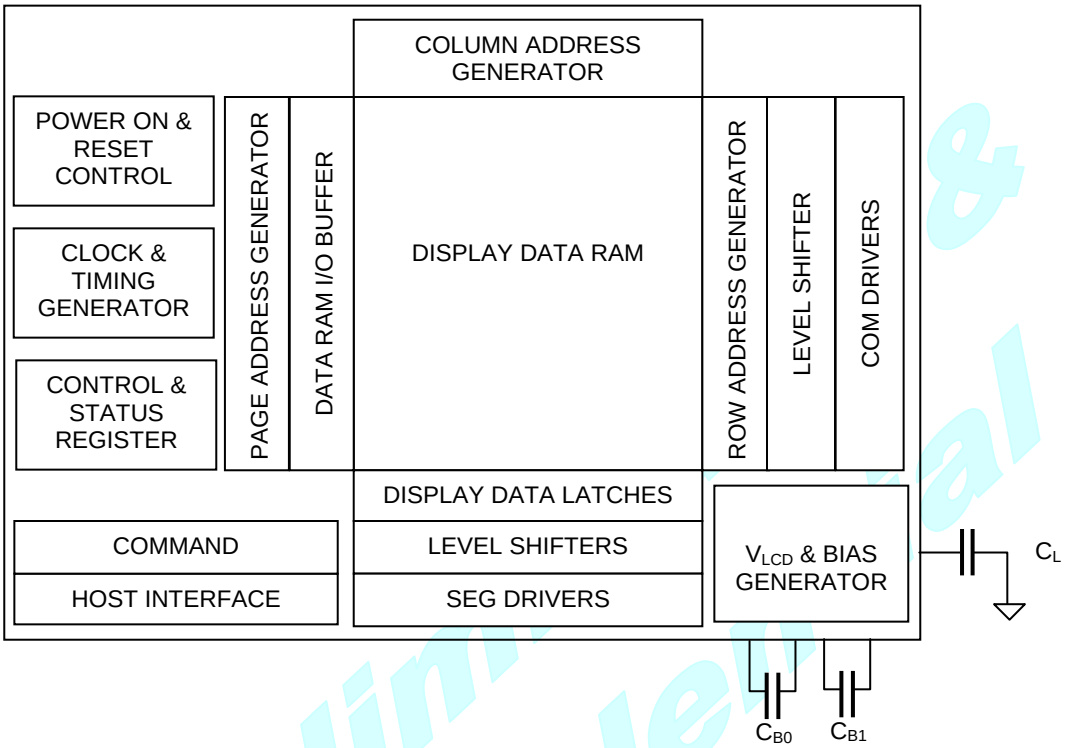
## BLOCK DIAGRAM



## PIN DESCRIPTION

| Name | Type | Pins | Description |
|---|---|---|---|
| **MAIN POWER SUPPLY** | | | |
| $V_{DD}$<br>$V_{DD2}$<br>$V_{DD3}$ | PWR | 1<br>2<br>1 | $V_{DD}$ is the digital power supply and it should be connected to a voltage source that is no higher than $V_{DD2}/V_{DD3}$.<br>$V_{DD2}/V_{DD3}$ is the analog power supply and it should be connected to the same power source.<br>Please maintain the following relationship:<br>$V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$<br>Minimize the trace resistance for $V_{DD}$ and $V_{DD2}/V_{DD3}$. |
| $V_{SS}$<br>$V_{SS2}$ | GND | 2<br>2 | Ground. Connect $V_{SS}$ and $V_{SS2}$ to the shared GND pin.<br>Minimize the trace resistance for $V_{SS}$ and $V_{SS2}$. |
| **LCD POWER SUPPLY & VOLTAGE CONTROL** | | | |
| $V_{B1+}$<br>$V_{B1-}$<br>$V_{B0+}$<br>$V_{B0-}$ | PWR | 2<br>2<br>2<br>2 | LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of $C_{BX}$ value between $V_{BX+}$ and $V_{BX-}$.<br>The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimizing the trace resistance is critical in achieving high quality image. |
| $V_{LCDIN}$<br>$V_{LCDOUT}$ | PWR | 1<br>1 | Main LCD Power Supply. Connect these pins together.<br>By-pass capacitor $C_L$ is optional. It can be connected between $V_{LCD}$ and $V_{SS}$. When $C_L$ is used, keep the trace resistance under 100 Ω. |

**NOTE**

- Recommended capacitor values:
  $C_B$: 150x ~ 250x LCD load capacitance or 2.2µF (2V), whichever is higher.
  $C_L$: 330nF (25V) is appropriate for most applications.

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0<br>BM1</td><td>I</td><td>1<br>1</td><td>Bus mode. The interface bus mode is determined by BM[1:0].
<table>
<tr><th>BM[1:0]</th><th>Mode</th></tr>
<tr><td>00</td><td>4 wire SPI w/ 8-bit token<br>(S8: conventional)</td></tr>
<tr><td>01</td><td>2-wire serial<br>($I^2C$)</td></tr>
<tr><td>10</td><td>3/4 wire SPI w/ 8-bit token<br>(S8uc: Ultra-compact)</td></tr>
<tr><td>11</td><td>3-wire SPI w/ 9-bit token<br>(S9: conventional)</td></tr>
</table></td></tr>
<tr><td>CS1<br>CS0</td><td>I</td><td>1<br>1</td><td>Chip Select or Chip Address. In S8 and S9 modes, chip is selected when CS0=”L” and CS1=”H”. When the chip is not selected, D[1:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1602s has built-in Power-On Reset and Software Reset command, RST pin is not required for proper chip operation.<br>An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to $V_{DD}$.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select the incoming command if it is a control instruction or for display data. CD pin is not used in S9 and $I^2C$ modes. Connect it to $V_{DD}$ or $V_{SS}$ then.<br>”L”: control instruction ”H”: display data</td></tr>
<tr><td>D0~D1</td><td>I/O</td><td>2</td><td>Bi-directional bus for both serial host interfaces.<br>In serial modes, connect D[0] to SCK, D[1] to SDA.<br>In COG applications, be careful to control ITO trace resistance, as it will affect effective output level of SDA.<br>Connect any unused pins to $V_{SS}$.</td></tr>
<tr><td colspan="4">HIGH VOLTAGE LCD DRIVER OUTPUT</td></tr>
<tr><td>SEG1 ~<br>SEG102</td><td>HV</td><td>102</td><td>SEG (column) driver outputs. Support up to 102 pixels.<br>Leave unused driver outputs open.</td></tr>
<tr><td>COM1 ~<br>COM64</td><td>HV</td><td>64</td><td>COM (row) driver outputs. Support up to 64 rows. Leave unused COM driver outputs open.</td></tr>
<tr><td>RIC</td><td>HV</td><td>2</td><td>Icon driver outputs. Leave it open if not used.</td></tr>
<tr><td colspan="4">MISC. PINS</td></tr>
<tr><td>$V_{DDX}$</td><td>O</td><td>2</td><td>Auxiliary $V_{DD}$. These pins are connected to the main $V_{DD}$ bus on chip. They are provided to facilitate chip configurations in COG applications.<br>These pins should not be used to provide $V_{DD}$ power to the chip. It is not necessary to connect $V_{DDX}$ to $V_{DD}$ externally.</td></tr>
<tr><td>TST4</td><td>I</td><td>1</td><td>Test control. Connect to GND.</td></tr>
<tr><td>TST2</td><td>I/O</td><td>1</td><td>Test I/O pins. Leave these pins open during normal use.</td></tr>
</table>

**Note:** Several control registers will specify the “0-based index” for COM and SEG electrodes. In those situations, COM*x* or SEG*x* will correspond to index *x*-1, and the value range for those index registers will be 0~64 for COM and 0~101 for SEG.

## RECOMMENDED COG LAYOUT



**NOTES FOR $V_{DD}$ WITH COG:**

The typical operation condition of UC1602s, $V_{DD}$=1.8V, should be met under all operating conditions. Unless $V_{DD}$ and $V_{DD2/3}$ ITO trances can each be controlled to be 20Ω or lower; otherwise $V_{DD}$-$V_{DD2/3}$ separation can cause the actual on-chip $V_{DD}$ to drop below $V_{DD}$=1.65V during high speed Data Write condition. Therefore, for COG, $V_{DD}$-$V_{DD2/3}$ separation requires very careful ITO layout and very stringent testing before MP.

## CONTROL REGISTERS

UC1602s contains registers that control the operation of the chip. These registers can be modified by software commands. The commands supported by UC1602s are described in the next section. The following table is a summary of all the registers defined by UC1602s and their default values.

*Name:* Symbolic reference of the register.
*Bits:* Number of bits in this register.
*Default:* Register value after the chip power up or system reset. The bold numbers show these defaults.
*Description:* Register meaning and functions.

| Name | Bits | Default | Description |
|---|---|---|---|
| SL | 6 | 0H | Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (63). Setting SL outside of this range causes undefined effect on the displayed image. |
| CA | 8 | 0H | Display Data RAM Column Address. Value range is **0**~101.<br>(Used Display Data RAM access from Host Interface) |
| PA | 4 | 0H | Display Data RAM Row Address (**0** ~ 7)<br>(Used in Host to Display Data RAM access) |
| BR | 2 | 3H | Bias Ratio. The ratio between $V_{LCD}$ and $V_{BIAS}$.<br>00: 6 01: 7<br>10: 8 **11: 9** |
| TC | 2 | 0H | Temperature Compensation (per °C).<br>**00b: 0.00%** 01b: -0.05%<br>10b: -0.10% 11b: -0.15% |
| PM | 8 | 62H | Electronic Potentiometer to fine tune the value of $V_{LCD}$ |
| PC | 3 | 6H | Power Control.<br>PC[0]: **0b: LCD: ⩽12nF**<br>1b: LCD: 12~20nF<br>PC[2:1]: 00b: External $V_{LCD}$<br>**11b: Internal $V_{LCD}$** (7x charge pump) |
| AC | 3 | 1H | Address Control:<br>AC[0]: WA: Automatic column/page Wrap Around (**Default 1: ON**)<br>AC[1]: Auto-Increment order<br>**0: Column (CA) first** 1: Page (PA) first<br>AC[2]: PID: PA (page address) auto Increment Direction (**L:+1** H:-1) |
| DC | 3 | 00H | Display Control:<br>DC[0]: PXV: Pixels Inverse (bit-wise data inversion. Default **0: OFF**)<br>DC[1]: APO: All Pixels ON (Default **0: OFF**)<br>DC[2]: Display ON/OFF (Default **0: OFF**) |
| LC | 6 | 10H | LCD Control:<br>LC[0]: MSF: MSB First mapping Option.<br>LC[1]: Reserved (always set 0)<br>LC[2]: MX, Mirror X. SEG/Column sequence inversion (Default: **OFF**)<br>LC[3]: MY, Mirror Y COM/Row sequence inversion (Default: **OFF**)<br>LC[4]: Line Rate = Frame-Rate x Mux-Rate<br>0b: 5.2 Klps **1b: 6.5 Klps**<br>(Klps: Kilo-line-per-second)<br>LC[5]: Partial Display<br>**0b: Disable**. Mux-Rate = CEN+1 (DST and DEN are not used.)<br>1b: Enable. Mux-Rate = DEN – DST +1 |
| RS | 1 | | Reset in progress. Host Interface not ready. |
| CEN<br>DST | 6<br>6 | 3FH<br>00H | COM scanning end (last COM with full line cycle, 0 based index)<br>Display start (first COM with active scan pulse, 0 based index) |

| Name | Bits | Default | Description |
|---|---|---|---|
| DEN | 6 | 3FH | Display end (last COM with active scan pulse, 0 based index)<br>Please maintain the following relationship:<br>CEN = (the actual number of pixel rows on the LCD) – 1<br>CEN ⩾ DEN ⩾ DST + 9 |
| APC | 1 | N/A | Advanced Program Control. For UltraChip only. Please do NOT use. |
| **STATUS REGISTER** | | | |
| OM | 2 | – | Operating Modes (read only)<br>00: Reset 01: (Not used)<br>10: Sleep 11: Normal |

## COMMAND TABLE

The following is a list of host commands supported by UC1602s

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
\# Useful Data bits
– Don't Care

| | Command | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Action | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Write Data Byte | 1 | 0 | # | # | # | # | # | # | # | # | Write 1 byte | N/A |
| 2 | Read Data Byte | 1 | 1 | # | # | # | # | # | # | # | # | Read 1 byte | N/A |
| 3 | Get Status | 0 | 1 | MX | MY | WA | DE | Product_ code[2:0] = 4H | | | Ver =0 | Get Status | N/A |
| 4 | Set Column Address LSB | 0 | 0 | 0 | 0 | 0 | 0 | # | # | # | # | Set CA [3:0] | 0H |
| | Set Column Address MSB | 0 | 0 | 0 | 0 | 0 | 1 | # | # | # | # | Set CA [6:4] | 0H |
| 5 | Set Temp. Compensation | 0 | 0 | 0 | 0 | 1 | 0 | 0 | - | # | # | Set TC[1:0] | 00b: 0.00%/°C |
| 6 | Set Power Control | 0 | 0 | 0 | 0 | 1 | 0 | 1 | # | # | # | Set PC[2:0] | 6H |
| 7 | Set Adv. Program Control<br>(double-byte command) | 0<br>0 | 0<br>0 | 0<br># | 0<br># | 1<br># | 1<br># | 0<br># | 0<br># | 0<br># | R<br># | Set APC[R][7:0], R = 0, or 1 | N/A |
| 8 | Set Scroll Line | 0 | 0 | 0 | 1 | # | # | # | # | # | # | Set SL[5:0] | 0H |
| 9 | Set Page Address | 0 | 0 | 1 | 0 | 1 | 1 | # | # | # | # | Set PA[3:0] | 0H |
| 10 | Set $V_{BIAS}$ Potentiometer<br>(double-byte command) | 0<br>0 | 0<br>0 | 1<br># | 0<br># | 0<br># | 0<br># | 0<br># | 0<br># | 0<br># | 1<br># | Set PM[7:0] | 62H |
| 11 | Set Partial Display Control | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | # | Set LC[5] | 0b |
| 12 | Set RAM Address Control | 0 | 0 | 1 | 0 | 0 | 0 | 1 | # | # | # | Set AC[2:0] | 1H |
| 13 | Set Line Rate | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | # | Set LC[4] | 1H |
| 14 | Set All-Pixel-ON | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | # | Set DC[1] | 0H |
| 15 | Set Inverse Display | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | # | Set DC[0] | 0H |
| 16 | Set Display Enable | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | # | Set DC[2] | 0H |
| 17 | Set LCD Mapping Control | 0 | 0 | 1 | 1 | 0 | 0 | # | # | 0 | # | Set LC[3:0] | 0H |
| 18 | System Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | System Reset | N/A |
| 19 | NOP | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | No operation | N/A |
| 20 | Set Test Control<br>(double-byte command) | 0<br>0 | 0<br>0 | 1<br># | 1<br># | 1<br># | 0<br># | 0<br># | 1<br># | TT<br># | | For testing only.<br>Do not use. | N/A |
| 21 | Set LCD Bias Ratio | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | # | # | Set BR[1:0] | 3H |
| 22 | Set COM End | 0 | 0 | 1<br>- | 1<br># | 1<br># | 1<br># | 0<br># | 0<br># | 0<br># | 1<br># | Set CEN[5:0] | 3FH |
| 23 | Set Partial Display start | 0 | 0 | 1<br>- | 1<br># | 1<br># | 1<br># | 0<br># | 0<br># | 1<br># | 0<br># | Set DST[5:0] | 00H |
| 24 | Set Partial Display End | 0 | 0 | 1<br>- | 1<br># | 1<br># | 1<br># | 0<br># | 0<br># | 1<br># | 1<br># | Set DEN[5:0] | 3FH |

* Other than commands listed above, all other bit patterns result in NOP (No Operation).

## COMMAND DESCRIPTION

### 1. Write Data Byte to Memory

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Write data | 1 | 0 | 8-bit Data write to SRAM | | | | | | | |

### 2. Read Data Byte from Memory

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Read data | 1 | 1 | 8-bit Data read from SRAM | | | | | | | |

Write/Read Data Byte (Command 1, or 2) accesses display data RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increase or decrease automatically after each bus cycle, depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of the page, and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches the end of the page, CA will be reset to 0 and PA will increase or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM, PA will be wrapped around to the other end of RAM and continue. (See command `Window Programming` for more details)

### 3. Get Status

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Get Status | 0 | 1 | MX | MY | WA | DE | Product_Code | | | Ver |

Status flag definitions:

*MX*: Status of register LC[1], mirror X.
*MY*: Status of register LC[2], mirror Y.
*WA:* Status of register AC[0]. Automatic column/row wrap around.
*DE*: Display enable flag. Display is enabled when DE=1.
*Product Code*: 100b
*Ver*: IC Version. **0** or 1.

### 4. Set Column Address

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Column Address LSB CA[3:0] | 0 | 0 | **0** | **0** | **0** | **0** | CA3 | CA2 | CA1 | CA0 |
| Set Column Address MSB CA[7:4] | 0 | 0 | **0** | **0** | **0** | **1** | - | CA6 | CA5 | CA4 |

Set the SRAM column address before Write/Read memory from host interface.

CA value range: **0**~101

### 5. Set Temperature Compensation

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Temperature Comp. TC[1:0] | 0 | 0 | **0** | **0** | **1** | **0** | **0** | **-** | TC1 | TC0 |

Set $V_{BIAS}$ temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

**00b= -0.00%/C** 01b= -0.05%/C 10b= -0.10%/C 11b= -0.15%/C

### 6. Set Power Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Multiplexing Rate PC[2:0] | 0 | 0 | **0** | **0** | **1** | **0** | **1** | PC2 | PC1 | PC0 |

Set PC[0] according to the capacitance loading of LCD panel.

**0b: LCD: ⩽ 12nF** 1b: LCD: 12~20nF

Set PC[2:1] to program the build-in charge pump stages:

00b: External $V_{LCD}$ **11b: Internal $V_{LCD}$** (7x charge pump)

### 7. Set Advanced Program Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Adv. Program Control APC[R][7:0] (Double-byte command) | 0 | 0 | **0** | **0** | **1** | **1** | **0** | **0** | **0** | R |
| | 0 | 0 | APC register parameter | | | | | | | |

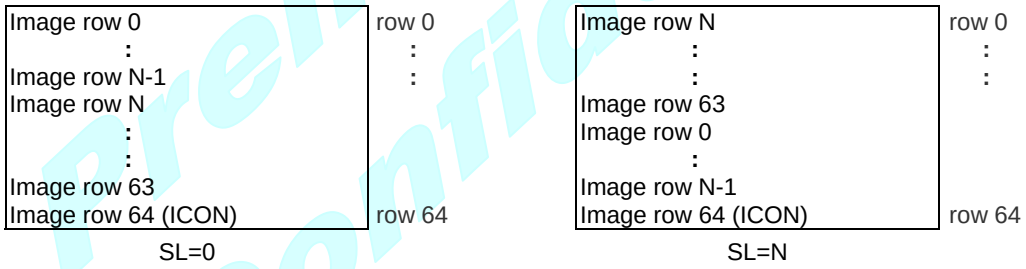
For UltraChip only. Please Do *NOT* use.

### 8. Set Scroll Line

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Scroll Line SL[5:0] | 0 | 0 | **0** | **1** | SL5 | SL4 | SL3 | SL2 | SL1 | SL0 |

Set the scroll line number. Possible value = **0**~63

Scroll line setting will scroll the displayed image up by *SL* rows.
Icon output RIC will not be affected by `Set Scroll Line` command.



### 9. Set Page Address

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Page Address | 0 | 0 | **1** | **0** | **1** | **1** | PA3 | PA2 | PA1 | PA0 |

Set the SRAM page address before write/read memory from host interface. Each page of SRAM corresponds to 8 COM lines on LCD panel, except for the last page. The last page corresponds to the icon output RIC.

Possible value = **0**~8.

### 10. Set $V_{BIAS}$ Potentiometer

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set $V_{BIAS}$ Potentiometer PM [7:0] (Double byte command) | 0 | 0 | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| | 0 | 0 | PM7 | PM6 | PM5 | PM4 | PM3 | PM2 | PM1 | PM0 |

Program $V_{BIAS}$ Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: 0 ~ 255

### 11. Set Partial Display Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set LC [5] | 0 | 0 | **1** | **0** | **0** | **0** | **0** | **1** | **0** | LC5 |

This command is used to enable partial display function.

L[5]: **0b Disable Partial Display**, Mux-Rate = CEN+1 (DST,DEN not used.)
1b Enable Partial Display, Mux-Rate = DEN - DST+1

### 12. Set RAM Address Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set AC [2:0] | 0 | 0 | **1** | **0** | **0** | **0** | **1** | AC2 | AC1 | AC0 |

Program registers AC[2:0] for RAM address control. It controls the auto-increment behavior of CA and PA.

AC[0] - WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
**1**: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or PA will increment by one step.

AC[1] – Auto-Increment order
**0** : column (CA) increment (+1) first until CA reach CA boundary, then PA will increment by (+/-1).
1 : page (PA) increment (+/-1) first until PA reach PA boundary, then CA will increment by (+1).

AC[2] – PID, page address (PA) auto increment direction ( **0**/1 = **+**/- 1 )
When WA=1 and CA reaches CA boundary, PID controls whether page address will be adjusted by +1 or –1.

### 13. Set Line Rate

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Line Rate LC [4] | 0 | 0 | **1** | **0** | **1** | **0** | **0** | **0** | **0** | LC4 |

Program LC [4] for frame rate setting

0b: 5.2Klps **1b: 6.5Klps**
(Klps: Kilo-line per second)

### 14. Set All Pixel ON

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set All Pixel ON DC [1] | 0 | 0 | **1** | **0** | **1** | **0** | **0** | **1** | **0** | DC1 |

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

### 15. Set Inverse Display

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Inverse Display DC [0] | 0 | 0 | **1** | **0** | **1** | **0** | **0** | **1** | **1** | DC0 |

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

### 16. Set Display Enable

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Display Enable DC[2] | 0 | 0 | **1** | **0** | **1** | **0** | **1** | **1** | **1** | DC2 |

This command is for programming register DC[2]. When DC[2] is set to 1, UC1602s will first exit from sleep mode, restore the power and then turn on COM drivers and SEG drivers.

### 17. Set LCD Mapping Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set LCD Control LC[3:0] | 0 | 0 | **1** | **1** | **0** | **0** | MY | MX | **0** | LC0 |

Set LC[3:2] for COM (row) mirror (MY), SEG (column) mirror (MX).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 50-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC[0]: MSF, MSB First mapping option.

### 18. System Reset

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| System Reset | 0 | 0 | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **0** |

This command will activate the system reset.

Control register values will be reset to their default values. Data store in RAM will not be affected.

### 19. NOP

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| No Operation | 0 | 0 | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **1** |

This command is used for “no operation”.

### 20. Set Test Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set TT | 0 | 0 | **1** | **1** | **1** | **0** | **0** | **1** | **TT** | |
| (Double byte command) | 0 | 0 | Testing parameter | | | | | | | |

This command is used for UltraChip production testing. Please do *NOT* use.

### 21. Set LCD Bias Ratio

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set Bias Ratio BR [1:0] | 0 | 0 | **1** | **1** | **1** | **0** | **1** | **0** | BR1 | BR0 |

Bias ratio definition:
00b= 6 01b= 7 10b= 8 **11b= 9**

### 22. Set COM End

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set COM | 0 | 0 | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **1** |
| (Double-byte command) | 0 | 0 | **-** | CEN register parameter | | | | | | |

This command programs the ending COM electrode.

CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-row in the LCD.

When the LCD has less than 64 pixel rows, the LCD designer should set CEN to N-1 (where N is the number of pixel rows) and use COM1 through COM-N as COM driver electrodes.

### 23. Set Partial Display Start

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set DST | 0 | 0 | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **0** |
| (Double-byte command) | 0 | 0 | **-** | DST register parameter | | | | | | |

This command programs the starting COM electrode. Which gas been assigned a full scanning period and will output an active COM scanning pulse.

### 24. Set Partial Display End

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Set DEN | 0 | 0 | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** |
| (Double-byte command) | 0 | 0 | **-** | DEN register parameter | | | | | | |

This command programs the ending COM electrode. Which gas been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

## LCD VOLTAGE SETTING

### MULTIPLEX RATES

Multiplex Rate (*MR*) is completely software programmable in UC1602s via the register MR.

The allowable LC[4] value is defined in the following table:

| MR | 0 | 1 |
|---|---|---|
| Line Rate | 5.2 | 6.5 |

**Table 1:** Bias Ratios

### BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between $V_{LCD}$ and $V_{BIAS}$, i.e.

*BR* = $V_{LCD}/V_{BIAS}$,
where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$, etc.

UC1602s supports four bias ratios (BR) as listed below. BR can be selected by software program.

| BR | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| Bias Ratio | 6 | 7 | 8 | 9 |

**Table 2:** Bias Ratios

The tunable range of $V_{BIAS}$ is from 0.8 V to 1.32 V at 25 $^{o}$C.

### $V_{BIAS}$ TEMPERATURE COMPENSATION

$V_{BIAS}$ is a temperature compensated reference voltage. $V_{BIAS}$ increases automatically as ambient temperature cools down.

For all four TC, $V_{BIAS}$ are normalized to a same voltage at 25 $^{o}$C. The compensation coefficients are given below:

| TC | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| % per $^{o}$C | 0.00 | - 0.05 | - 0.10 | - 0.15 |

**Table 3:** Temperature Compensation

### $V_{LCD}$ GENERATION

$V_{LCD}$ may be supplied either by internal charge pump or by external power supply. The source of $V_{LCD}$ is controlled by PC[2:1]. For good product reliability, it is recommended to keep $V_{LCD}$ under 11.5 V for all temperature conditions.

When $V_{LCD}$ is generated internally, the voltage level of $V_{LCD}$ is determined by four control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

$C_{V0}$ and $C_{PM}$ are two design constants. The values are provided in the Figure on the next page,

$PM$ is the numerical value of PM register,

$T$ is the ambient temperature in $^{O}$C, and

$C_T$ is the temperature compensation coefficient as selected by TC register.

### $V_{LCD}$ FINE TUNING

Black-and-white STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the $V_{OP}$ of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust $V_{LCD}$ to match the actual $V_{OP}$ of the LCD.

For the best result, software based approach for $V_{LCD}$ adjustment is the recommended method for $V_{LCD}$ fine-tuning.

For applications where mechanical manual fine-tuning of $V_{LCD}$ becomes necessary, then $V_{BIAS}$ pin may be used with an external trim pot to fine tune the $V_{LCD}$. Please refer to Application Notes for more detailed discussion on this subject.

### LOAD DRIVING STRENGTH

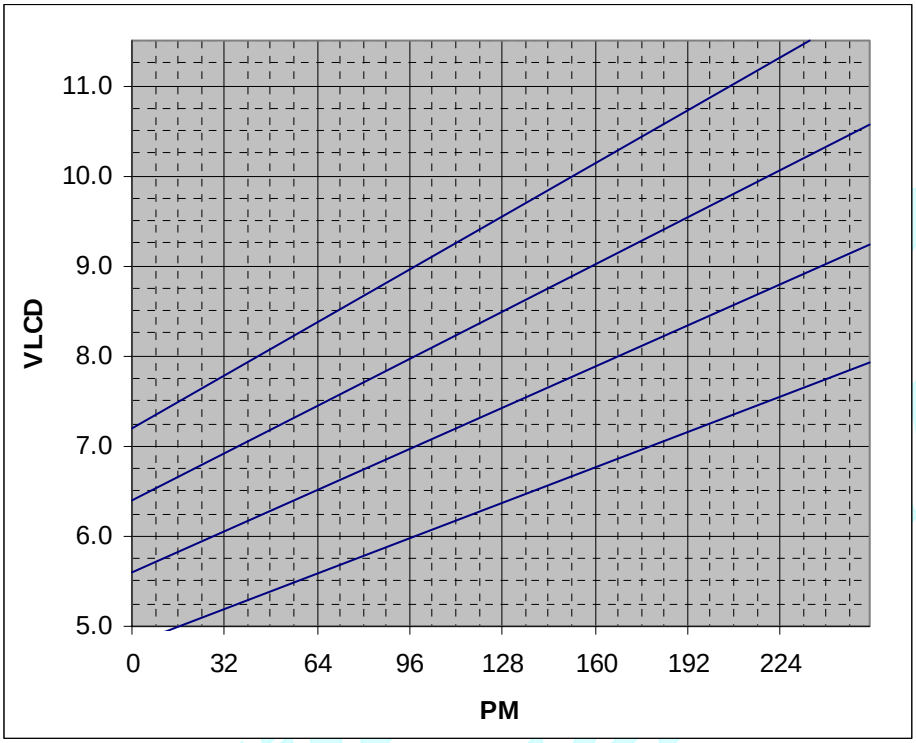
UC1602s' power supply circuits are designed to handle LCD panels with load capacitance up to ~30nF when $V_{DD2}$ = 2.5V, and up to ~35nF when $V_{DD2} \geq$ 3V.

### POWER UP/DOWN SEQUENCE

Due to the use of fully embedded power supply, built-in power ready detector, and draining circuit, there is no explicit power up, power down sequences for UC1602s controllers when using internal $V_{LCD}$ generator.

On the other hand, caution must be exercised when external $V_{LCD}$ source is used. The general rule of thumb is to make sure Display Enable is OFF before connecting or disconnecting external $V_{LCD}$ sources.

## $V_{LCD}$ QUICK REFERENCE




$V_{LCD}$ Programming Curve.

| BR | $C_{V0}$ (V) | $C_{PM}$ (mV) | PM | $V_{LCD}$ Range (V) |
|---|---|---|---|---|
| 6 | 4.8 | 12.24 | 0 | 4.8 |
| | | | 255 | 7.92 |
| 7 | 5.6 | 14.28 | 0 | 5.6 |
| | | | 255 | 9.24 |
| 8 | 6.4 | 16.32 | 0 | 6.4 |
| | | | 255 | 10.56 |
| 9 | 7.2 | 18.36 | 0 | 7.2 |
| | | | 234 | 11.5 |

**Note:**

The maximum reliable $V_{LCD}$ operating value is at 11.5V. For best reliability, keep $V_{LCD}$ under **11.5V** under all temperature.

### HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

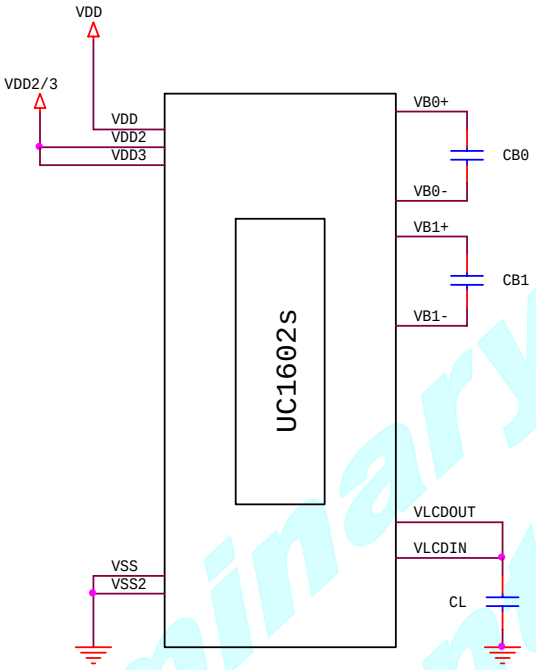



**FIGURE 1:** Reference circuit using internal Hi-V generator circuit

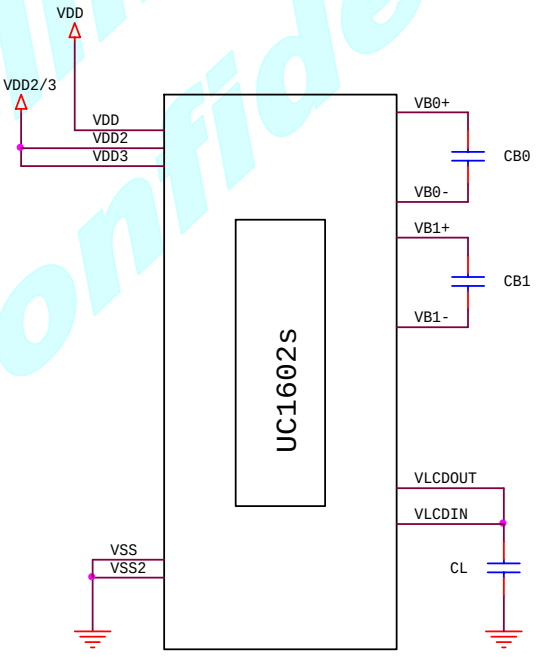



**FIGURE 2:** Reference circuit using external Hi-V source

**Note**

- Recommended component values:
  $C_B$: 150x~250x LCD load capacitance or 2.2uF (2V), whichever is higher.
  $C_L$: 330nF (25V) is appropriate for most applications.

## LCD DISPLAY CONTROLS

### CLOCK & TIMING GENERATOR

UC1602s contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Two different line rates are provided for system design flexibility: 5.2 Klps and 6.5 Klps.

Choose lower line rate for lower power, and choose higher line rate to improve LCD contrast and minimize flicker.

### DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG and COM drivers are in idle mode, their outputs are connected to $V_{SS}$.

### DRIVER ARRANGEMENTS

The naming conventions are: COM*x* (where x = 1~64) refers to the row driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, MX or MY settings.

### DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

### DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display ON* command. When DC[2] is set to OFF (logic “0”), both column and row drivers will become idle and UC1602s will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”,and UC1602s will first exit from Sleep Mode, restore the power ($V_{LCD}$, $V_{BIAS}$ etc.) and then turn on row drivers and proper column drivers.

#### ALL PIXELS ON (APO)

When set, this flag will force all active column drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

#### INVERSE (PXV)

When this flag set to ON, active column drivers will output the inverse of the value it received from the display buffer RAM. This flag has no impact on data stored in RAM.

#### PARTIAL SCROLL

Control register FL specifies a region of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can used to implement fixed region when the other part of the display is scrolled by SL.

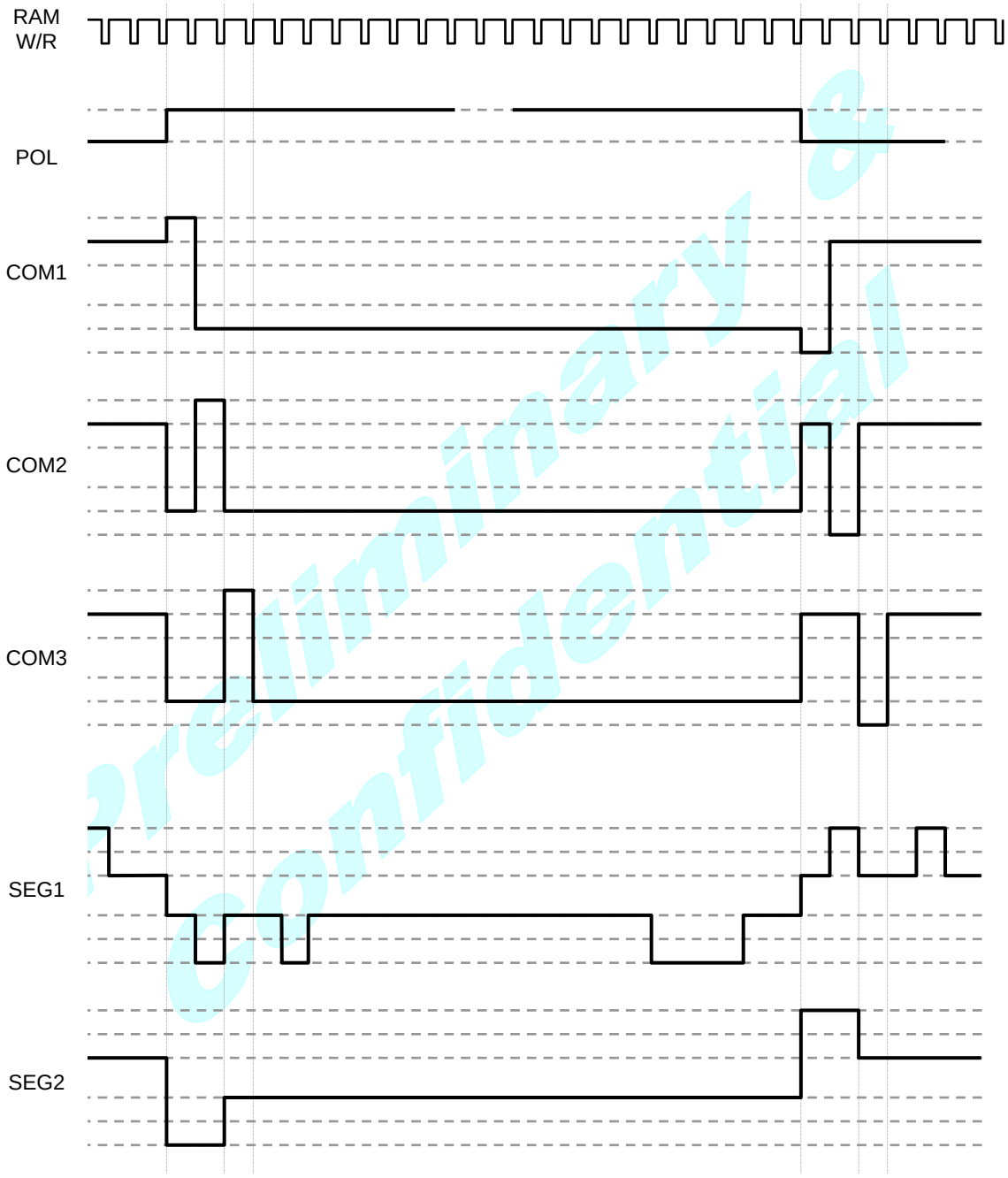



**FIGURE 3:** COM and SEG Electrode Driving Waveform

## HOST INTERFACE

As summarized in the table below, UC1602s supports four serial bus protocols, which designers can use to create compact LCD modules.

| | | Bus Type | | | |
|---|---|---|---|---|---|
| | | **S8 (4wr)** | **S8uc (3wr)** | **S9** | **$I^2C$** |
| Control & Data Pins | Width | Serial | | | |
| | Access | Write Only | | | R / W |
| | BM[1:0] | 0 | 10 | 11 | 01 |
| | CS[1:0] | Chip Select | - | Chip Select | - |
| | CD | Control / Data | | – | |
| | D[1:0] | D0=SCK, D1=SDA | | | |

* Connect unused control pins and data bus pins to $V_{DD}$ or $V_{SS}$.

**Table 4:** Host Interfaces Choices

### SERIAL INTERFACE

UC1602s supports four serial modes, one 4-wire SPI mode (S8), one compact 3/4-wire mode (S8uc), one 3-wire SPI mode (S9), and one 2-wire SPI mode (I2C). Bus interface mode is determined by the wiring of the BM[1:0]. See table in last page for more detail.

#### 4-wire Serial Interface (S8)

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

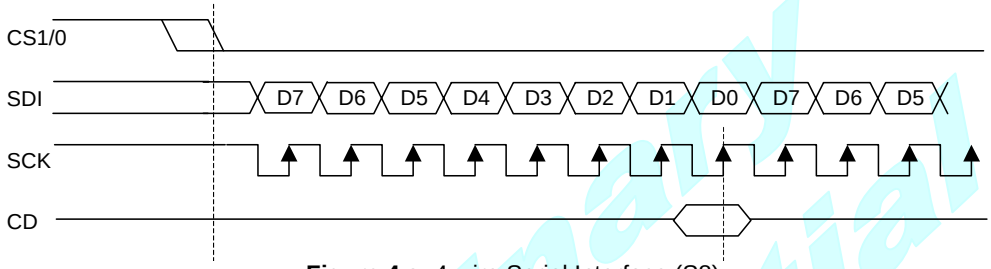



**Figure 4.a:** 4-wire Serial Interface (S8)

### S8UC (3/4-WIRE) INTERFACE

Only write operations are supported in this 3/4-wire serial mode. The data format is identical to S8. However, in addition to CS pins, CD pin transitions will also reset the bus cycle in this mode. So, if CS pins are hardwired to enable chip-select, the bus can work properly with only three signal pins.

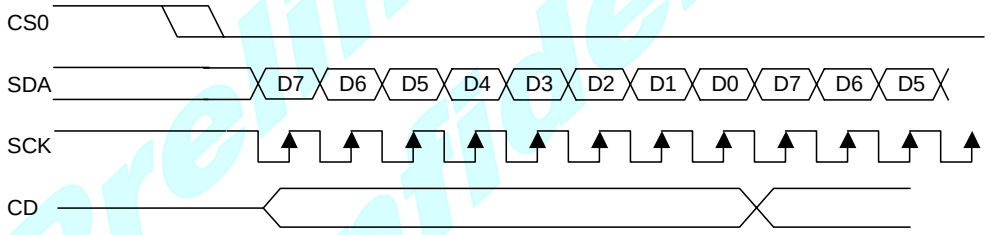



**FIGURE 4.b:** 3/4-wire Serial Interface (S8uc)

### S9 (3-WIRE) INTERFACE

Only write operations are supported in this 3-wire serial mode. Pins CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either $V_{DD}$ or $V_{SS}$. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

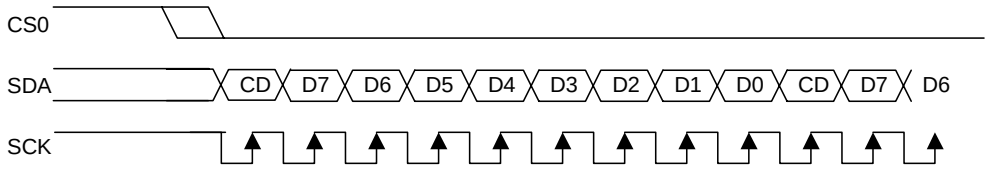



**FIGURE 4.c:** 3-wire Serial Interface (S9)

### 2-WIRE SERIAL INTERFACE ($I^2C$)

When BM[1:0] is set to “LH”, UC1602s is configured as a $I^2C$ Bus signaling protocol compliant slave device. Please refer to $I^2C$ standard for details of the bus signaling protocol. Please refer to AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and is used to configure UC1602s' device address. Proper wiring to $V_{DD}$ or $V_{SS}$ is required for the IC to operate properly for $I^2C$ mode.

Each UC1602s $I^2C$ interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in $I^2C$ mode and should be connected to $V_{SS}$.

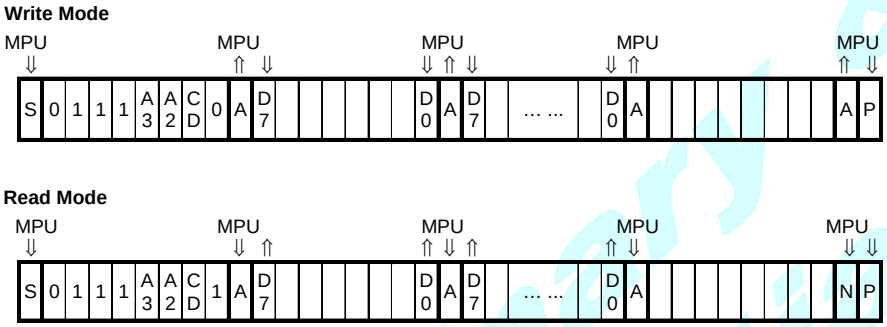


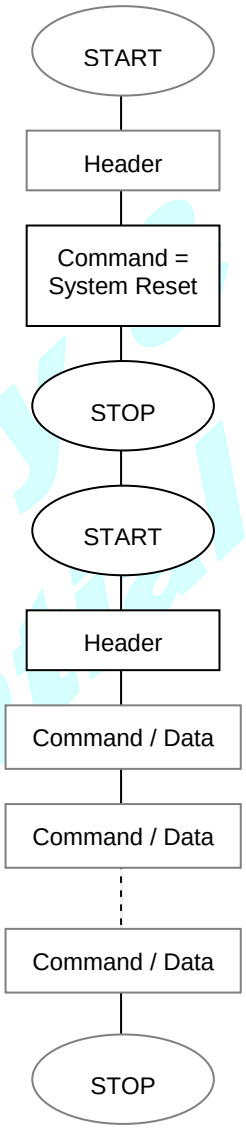

**Figure 4.d:** 2-wire Serial Interface ($I^2C$)

The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1602s will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1602s) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the bus master.

When using $I^2C$ serial mode, if the command of System Reset is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a “System Reset” command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.




Writing sequence with System Reset

## HOST INTERFACE REFERENCE CIRCUIT

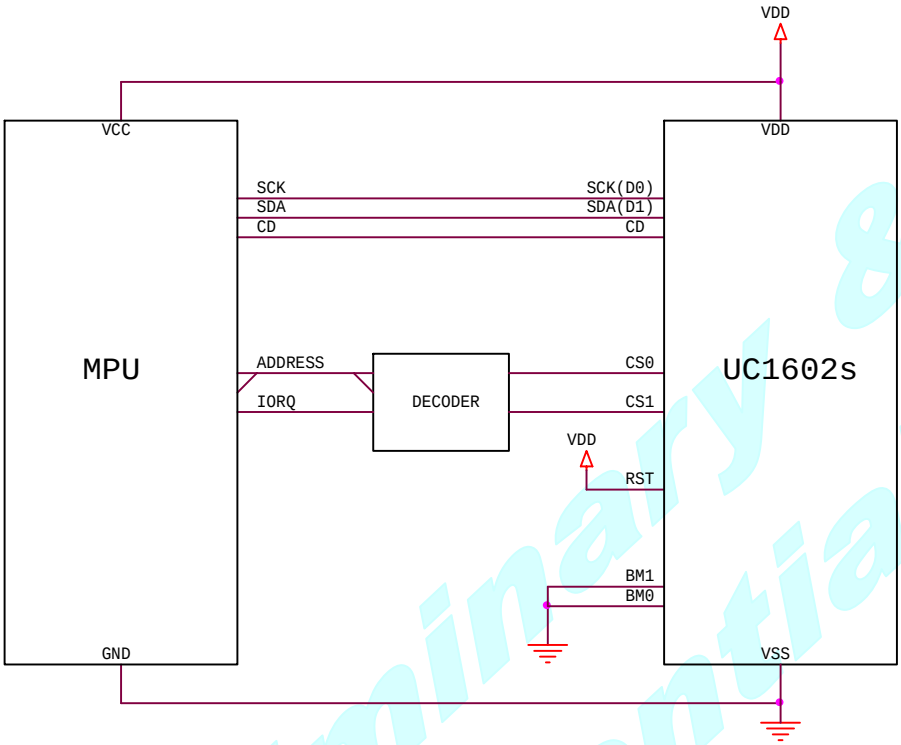



**FIGURE 5:** 4-wire SPI (S8) serial mode reference circuit

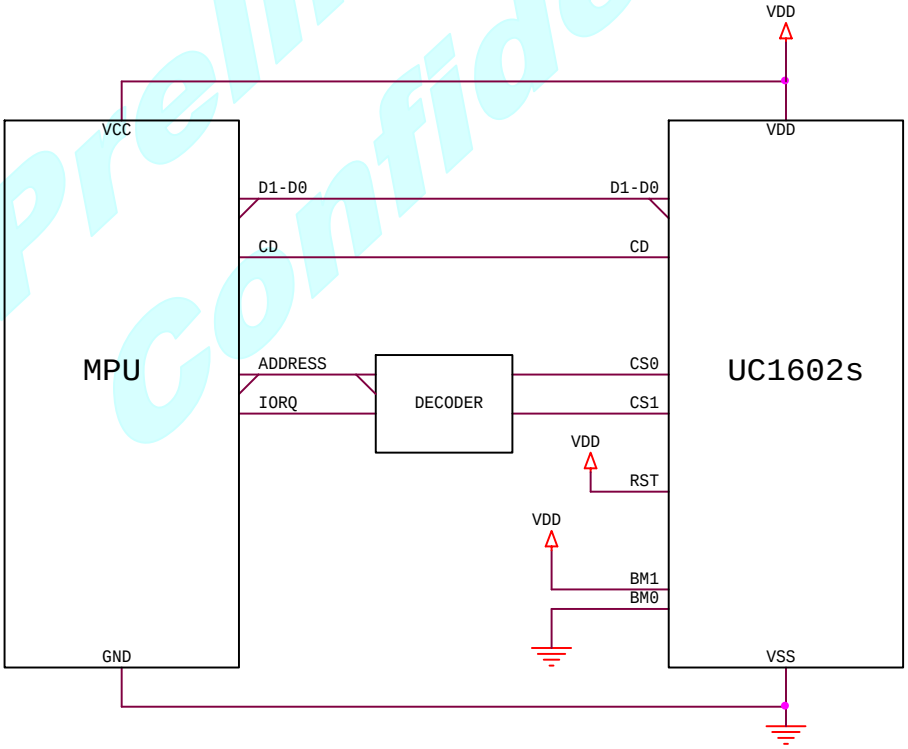



**FIGURE 6:** 3 / 4 -wire SPI (S8uc) serial mode reference circuit

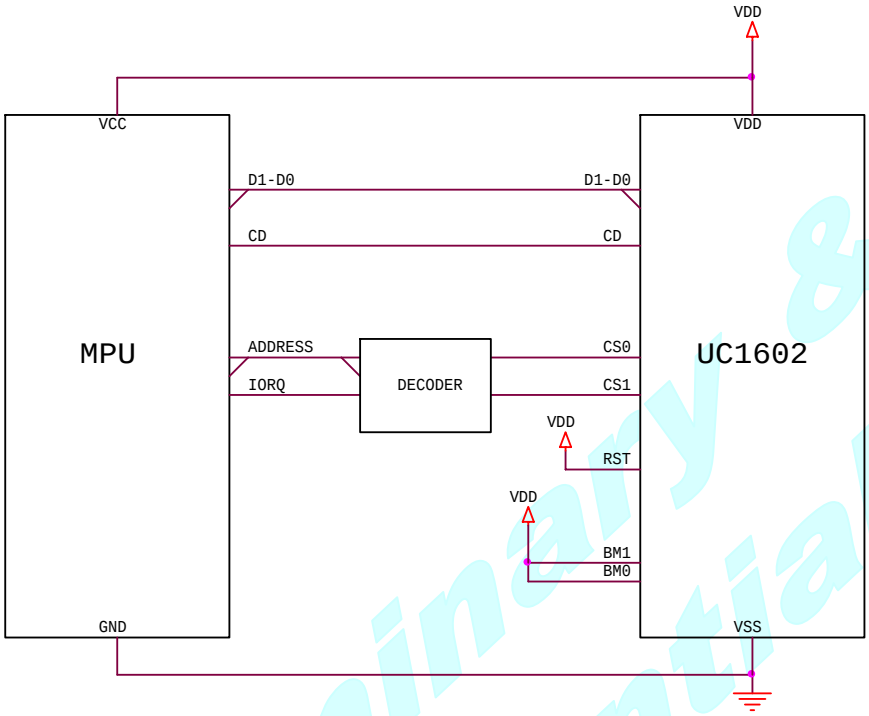



**FIGURE7:** 3-wire SPI (S9) serial mode reference circuit

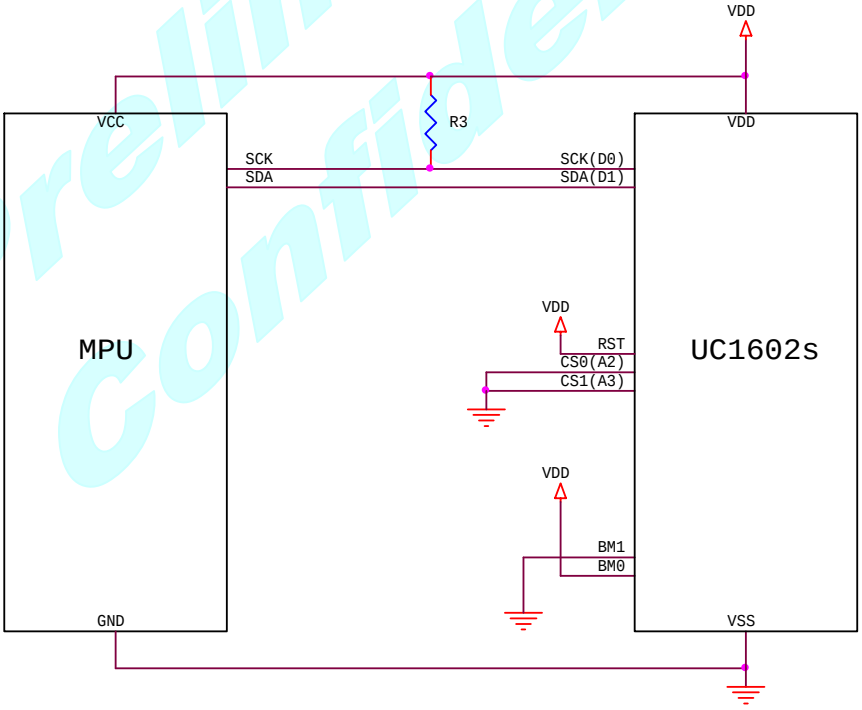



**FIGURE 8:** 2-wire SPI ($I^2C$) serial mode reference circuit

**Note:**
1. RST pin is optional. When RST pin is not used, connect the pin to $V_{DD}$.
2. R3: 2k ~ 10k Ω, use lower resistor for bus speed up to 3.6MHz, use higher resistor for lower power.

# DISPLAY DATA RAM

### DATA ORGANIZATION

The input display data is stored to a dual port static RAM (RAM, for Display Data RAM) organized as 65x102.

After setting CA and RA, the subsequent data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page among the relations of COM, SEG, SRAM, and various memory control registers.

### DISPLAY DATA RAM ACCESS

The Display Data RAM is a special purpose dual port RAM, which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

### DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (101), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 7), PA will be wrapped around to the other end of RAM and continue.

### MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (101 - CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

### ROW SCANNING

For each field, the scanning starts at R1 through R*m*, where *m* depends on the setting of MR.

Row electrode scanning orders are not affected by Start Line (SL), or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

### RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed R*m* scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
*Line* = *SL*

Otherwise
*Line* = Mod(*Line*+1, 64)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produce the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches *64*.

### MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
*Line* = Mod(*SL* + *MR -1*, *64*)
Otherwise

*Line* = Mod(*Line-1* , *64*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

| PA[3:0] | 0 | Line AddeCss | Page | MY=0 SL=0 | MY=0 SL=16 | MY=1 SL=0 | MY=1 SL=0 | MY=1 SL=25 | MY=1 SL=25 |
|---|---|---|---|---|---|---|---|---|---|
| 0000 | D0 | 00H | Page 0 | C1 | C49 | C64 | C48 | C25 | C9 |
| | D1 | 01H | | C2 | C50 | C63 | C47 | C24 | C8 |
| | D2 | 02H | | C3 | C51 | C62 | C46 | C23 | C7 |
| | D3 | 03H | | C4 | C52 | C61 | C45 | C22 | C6 |
| | D4 | 04H | | C5 | C53 | C60 | C44 | C21 | C5 |
| | D5 | 05H | | C6 | C54 | C59 | C43 | C20 | C4 |
| | D6 | 06H | | C7 | C55 | C58 | C42 | C19 | C3 |
| | D7 | 07H | | C8 | C56 | C57 | C41 | C18 | C2 |
| 0001 | D0 | 08H | Page 1 | C9 | C57 | C56 | C40 | C17 | C1 |
| | D1 | 09H | | C10 | C58 | C55 | C39 | C16 | --- |
| | D2 | 0AH | | C11 | C59 | C54 | C38 | C15 | --- |
| | D3 | 0BH | | C12 | C60 | C53 | C37 | C14 | --- |
| | D4 | 0CH | | C13 | C61 | C52 | C36 | C13 | --- |
| | D5 | 0DH | | C14 | C62 | C51 | C35 | C12 | --- |
| | D6 | 0EH | | C15 | C63 | C50 | C34 | C11 | --- |
| | D7 | 0FH | | C16 | C64 | C49 | C33 | C10 | --- |
| 0010 | D0 | 10H | Page 2 | C17 | C1 | C48 | C32 | C9 | --- |
| | D1 | 11H | | C18 | C2 | C47 | C31 | C8 | --- |
| | D2 | 12H | | C19 | C3 | C46 | C30 | C7 | --- |
| | D3 | 13H | | C20 | C4 | C45 | C29 | C6 | --- |
| | D4 | 14H | | C21 | C5 | C44 | C28 | C5 | --- |
| | D5 | 15H | | C22 | C6 | C43 | C27 | C4 | --- |
| | D6 | 16H | | C23 | C7 | C42 | C26 | C3 | --- |
| | D7 | 17H | | C24 | C8 | C41 | C25 | C2 | --- |
| 0011 | D0 | 18H | Page 3 | C25 | C9 | C40 | C24 | C1 | --- |
| | D1 | 19H | | C26 | C10 | C39 | C23 | C64 | C48* |
| | D2 | 1AH | | C27 | C11 | C38 | C22 | C63 | C47 |
| | D3 | 1BH | | C28 | C12 | C37 | C21 | C62 | C46 |
| | D4 | 1CH | | C29 | C13 | C36 | C20 | C61 | C45 |
| | D5 | 1DH | | C30 | C14 | C35 | C19 | C60 | C44 |
| | D6 | 1EH | | C31 | C15 | C34 | C18 | C59 | C43 |
| | D7 | 1FH | | C32 | C16 | C33 | C17 | C58 | C42 |
| 0100 | D0 | 20H | Page 4 | C33 | C17 | C32 | C16 | C57 | C41 |
| | D1 | 21H | | C34 | C18 | C31 | C15 | C56 | C40 |
| | D2 | 22H | | C35 | C19 | C30 | C14 | C55 | C39 |
| | D3 | 23H | | C36 | C20 | C29 | C13 | C54 | C38 |
| | D4 | 24H | | C37 | C21 | C28 | C12 | C53 | C37 |
| | D5 | 25H | | C38 | C22 | C27 | C11 | C52 | C36 |
| | D6 | 26H | | C39 | C23 | C26 | C10 | C51 | C35 |
| | D7 | 27H | | C40 | C24 | C25 | C9 | C50 | C34 |
| 0101 | D0 | 28H | Page 5 | C41 | C25 | C24 | C8 | C49 | C33 |
| | D1 | 29H | | C42 | C26 | C23 | C7 | C48 | C32 |
| | D2 | 2AH | | C43 | C27 | C22 | C6 | C47 | C31 |
| | D3 | 2BH | | C44 | C28 | C21 | C5 | C46 | C30 |
| | D4 | 2CH | | C45 | C29 | C20 | C4 | C45 | C29 |
| | D5 | 2DH | | C46 | C30 | C19 | C3 | C44 | C28 |
| | D6 | 2EH | | C47 | C31 | C18 | C2 | C43 | C27 |
| | D7 | 2FH | | C48 | C32 | C17 | C1 | C42 | C26 |
| 0110 | D0 | 30H | Page 6 | C49 | C33 | C16 | --- | C41 | C25 |
| | D1 | 31H | | C50 | C34 | C15 | --- | C40 | C24 |
| | D2 | 32H | | C51 | C35 | C14 | --- | C39 | C23 |
| | D3 | 33H | | C52 | C36 | C13 | --- | C38 | C22 |
| | D4 | 34H | | C53 | C37 | C12 | --- | C37 | C21 |
| | D5 | 35H | | C54 | C38 | C11 | --- | C36 | C20 |
| | D6 | 36H | | C55 | C39 | C10 | --- | C35 | C19 |
| | D7 | 37H | | C56 | C40 | C9 | --- | C34 | C18 |
| 0111 | D0 | 38H | Page 7 | C57 | C41 | C8 | --- | C33 | C17 |
| | D1 | 39H | | C58 | C42 | C7 | --- | C32 | C16 |
| | D2 | 3AH | | C59 | C43 | C6 | --- | C31 | C15 |
| | D3 | 3BH | | C60 | C44 | C5 | --- | C30 | C14 |
| | D4 | 3CH | | C61 | C45 | C4 | --- | C29 | C13 |
| | D5 | 3DH | | C62 | C46 | C3 | --- | C28 | C12 |
| | D6 | 3EH | | C63 | C47 | C2 | --- | C27 | C11 |
| | D7 | 3FH | | C64 | C48 | C1 | --- | C26 | C10 |
| 1000 | D0 | 40H | Page 8 | CIC | CIC | CIC | CIC | CIC | CIC |
| | | | | | | 65 | 49 | 65 | 49 |
| | | | | | | | MUX | | |


Example for memory mapping: let MX = 0, MY = 0, SL = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1: 00011111b

⇒ Page 0 SEG 2: 11001100b

## RESET & POWER MANAGEMENT

### TYPES OF RESET

UC1602s has two different types of Reset:

*Power-ON-Reset* and *System-Reset*.

*Power-ON-Reset* is performed right after $V_{DD}$ is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for $V_{DD}$ to stabilize, and then trigger the *System Reset*.

*System Reset* can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

### RESET STATUS

When UC1602s enters RESET sequence:

- Operation mode will be “Reset”
- System Status bit RS will stay as “1” until the Reset process is completed. When RS=1, the IC will only respond to *Get Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

### OPERATION MODES

UC1602s has three operating modes (OM):
Reset, Sleep, Normal.

For each mode, the related statuses are as below:

| Mode | Reset | Sleep | Normal |
|---|---|---|---|
| OM | 00 | 10 | 11 |
| Host Interface | Active | Active | Active |
| Clock | OFF | OFF | ON |
| LCD Drivers | OFF | OFF | ON |
| Charge Pump | OFF | OFF | ON |
| Draining Circuit | ON | ON | OFF |

**Table 5:** Operating Modes

### CHANGING OPERATION MODE

Two commands will initiate OM transitions:
*Set Display Enable*, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter power saving mode.

OM changes are synchronized with the edges of UC1602s internal clock. To ensure consistent system states, wait at least 10μS after *Set Display Enable or System Reset* command.

| Action | Mode | OM |
|---|---|---|
| Reset command<br>RST_ pin pulled “L”<br>Power ON reset | Reset | 00 |
| Set Driver Enable to “0” | Sleep | 10 |
| Set Driver Enable to “1” | Normal | 11 |

**Table 6:** OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors $C_{B0}$, $C_{B1}$, and $C_L$. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1602s consumes very little energy in Sleep mode (typically under 2μA).

### EXITING SLEEP MODE

UC1602s contains internal logic to check whether $V_{LCD}$ and $V_{BIAS}$ are ready before releasing row and column drivers from their OFF states. When exiting Sleep Mode and Reset Mode, column and row drivers will not be activated until UC1602s internal voltage sources are restored to their proper values.

### POWER-UP SEQUENCE

UC1602s power-up sequence is simplified by built-in "Power Ready" flags and by the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 5~10 mS before CPU starting to issue commands to UC1602s. No additional time sequences are required for enabling of the charge pump, turning on the display drivers and writing to RAM or any other commands. However, while turning on $V_{DD}$, $V_{DD2/3}$ should be started not later than $V_{DD}$.

Delay allowance between $V_{DD}$ and $V_{DD2/3}$ is illustrated as Figure 11.

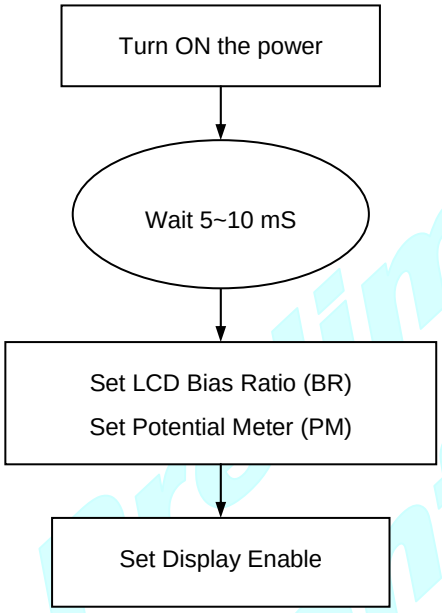



**FIGURE 9:** Reference Power-Up Sequence

### POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors $C_{BX+}$, $C_{BX-}$, and $C_{LCD}$ from damaging the LCD when $V_{DD}$ is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

The draining resistance is 3K Ω for both $V_{LCD}$ and $V_{B+}$. It is recommended to wait *3* x *RC* for $V_{LCD}$ and *1.5 x RC* for $V_{B+}$. For example, if $C_{LCD}$ is 330nF, then the draining time required for $V_{LCD}$ is 0.5~1mS.

When internal $V_{LCD}$ is not used, UC1602s will *not* drain $V_{LCD}$ during RESET. System designers need to make sure external $V_{LCD}$ source is properly drained off before turning off $V_{DD}$.

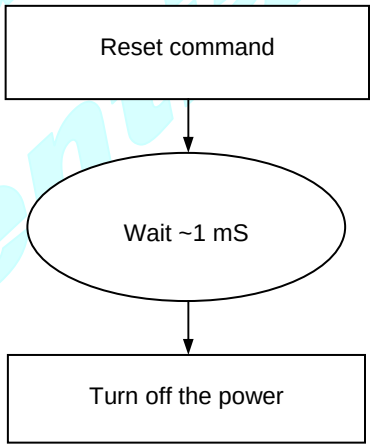



**FIGURE 10:** Reference Power-Down Sequence

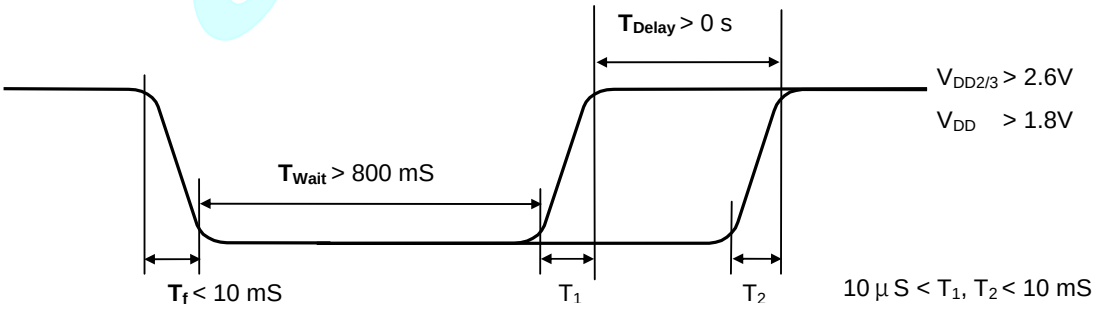



**Figure 11:** Delay allowance and Power Off-On Sequence

### SAMPLE COMMAND SEQUENCES FOR POWER MANAGEMENT

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)
Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

#### POWER-UP

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | – | – | – | – | – | – | – | – | – | – | Automatic Power-ON Reset. | Wait ~5mS after $V_{DD}$ is ON |
| C | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | # | # | (5) Set Temp. Compensation | Set up LCD format specific parameters, MX, MY, etc. |
| C | 0 | 0 | 1 | 1 | 0 | 0 | 0 | # | # | # | (17) Set LCD Mapping Control | |
| A | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | # | (13) Set Line Rate | Fine tune for power, flicker, contrast. |
| C | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | # | # | (21) Set LCD Bias Ratio | LCD specific operating voltage setting |
| R | 0<br>0 | 0<br>0 | 1<br># | 0<br># | 0<br># | 0<br># | 0<br># | 0<br># | 0<br># | 1<br># | (10) Set $V_{BIAS}$ Potentiometer | |
| O | 1<br>.<br>.<br>1 | 0<br>.<br>.<br>0 | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | Write display RAM | Set up display image |
| R | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | (16) Set Display Enable | |

#### POWER-DOWN

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | (18) System Reset | |
| R | – | – | – | – | – | – | – | – | – | – | Draining capacitor | Wait ~1mS before $V_{DD}$ OFF |

#### DISPLAY-OFF

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | (16) Set Display Disable | |
| C | 1<br>.<br>.<br>1 | 0<br>.<br>.<br>0 | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | #<br>.<br>.<br># | Write display RAM | Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.) |
| R | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | (16) Set Display Enable | |

## ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is, therefore, highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1602s require special "ESD Sensitivity" consideration in particular:

| Test Mode / Pin Name | MM* $V_{DD}$ | MM* $V_{SS}$ | HBM* $V_{DD}$ | HBM* $V_{SS}$ |
|---|---|---|---|---|
| VB1+ | (TBD) | | | |
| VB1- | | | | |
| VB0+ | | | | |
| VB0- | | | | |
| $V_{LCDIN}/_{OUT}$ | | | | |
| COM/SEG Driver pins | | | | |

* MM: Machine Mode; HBM: Human Body Mode

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

## ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134 - notes 1, 2 and 3.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Logic Supply voltage | -0.3 | +4.0 | V |
| $V_{DD2}$ | LCD Generator Supply voltage | -0.3 | +4.0 | V |
| $V_{DD3}$ | Analog Circuit Supply voltage | -0.3 | +4.0 | V |
| $V_{DD2/3}$-$V_{DD}$ | Voltage difference between $V_{DD}$ and $V_{DD2/3}$ | -- | 1.6 | V |
| $V_{LCD}$ | LCD Generated voltage | -0.3 | +13.2 | V |
| $V_{IN}$ / $V_{OUT}$ | Any input/output | -0.4 | $V_{DD}$ + 0.3 | V |
| $T_{OPR}$ | Operating temperature range | -30 | +85 | $^{o}$C |
| $T_{STR}$ | Storage temperature | -55 | +125 | $^{o}$C |

### Notes

1. $V_{DD}$ is based on $V_{SS}$ = 0V
2. Stress values listed above may cause permanent damages to the device.

## SPECIFICATIONS

### DC CHARACTERISTICS

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply for digital circuit | | 1.65 | | 3.45 | V |
| $V_{DD2/3}$ | Supply for bias & pump | | 2.5 | | 3.45 | V |
| $V_{LCD}$ | Charge pump output | $V_{DD2/3} \geqslant 2.6V$, $25^{O}C$ | | | 11.5 | V |
| $V_D$ | LCD data voltage | $V_{DD2/3} \geqslant 2.6V$, $25^{O}C$ | 0.80 | | 1.32 | V |
| $V_{IL}$ | Input logic LOW | | | | $0.2V_{DD}$ | V |
| $V_{IH}$ | Input logic HIGH | | $0.8V_{DD}$ | | | V |
| $V_{OL}$ | Output logic LOW | | | | $0.2V_{DD}$ | V |
| $V_{OH}$ | Output logic HIGH | | $0.8V_{DD}$ | | | V |
| $I_{IL}$ | Input leakage current | | | | 1.5 | μA |
| $R_{0(SEG)}$ | SEG output impedance | $V_{LCD}$ = 11V | | 2 | 3 | kΩ |
| $R_{0(COM)}$ | COM output impedance | $V_{LCD}$ = 11V | | 2 | 3 | kΩ |
| $F_{FR}$ | Average Frame Rate | LC[3] = 0b | -10% | 80 | +10% | Hz |

### POWER CONSUMPTION

$V_{DD}$ = (TBD) V,
$V_{LCD}$ = (TBD)V
Mux Rate = (TBD),
$C_B$ = (TBD) μF

Bias Ratio = (TBD)b,
Frame Rate = (TBD)b,
Bus mode = (TBD),
Temperature = (TBD),

PM = (TBD),
Panel Loading (PC[0]) ⩽ (TBD),
$C_L$ = (TBD) nF,
All outputs are open circuit.

| Display Pattern | Conditions | Typ. | Max. |
|---|---|---|---|
| All-OFF | Bus = idle | (TBD) | (TBD) |
| 2-pixel checker | Bus = idle | (TBD) | (TBD) |
| - | Bus = idle (standby current) | - | 5 |

## AC CHARACTERISTICS

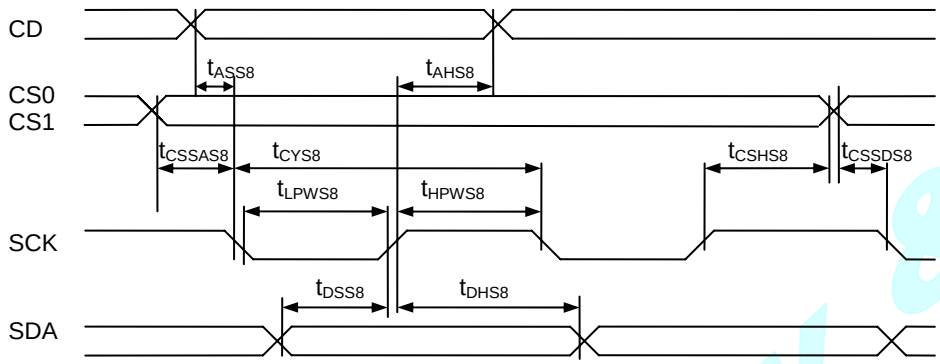



**FIGURE 12:** Serial Bus Timing Characteristics (for S8 / S8uc)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{ASS8}$ | CD | Address setup time | | 0 | – | nS |
| $t_{AHS8}$ | | Address hold time | | 40 | – | nS |
| $t_{CYS8}$ | SCK | System cycle time | | 135 | – | nS |
| $t_{LPWS8}$ | | Low pulse width | | 65 | – | nS |
| $t_{HPWS8}$ | | High pulse width | | 65 | – | nS |
| $t_{DSS8}$<br>$t_{DHS8}$ | SDA | Data setup time<br>Data hold time | | 30<br>15 | – | nS |
| $t_{CSSAS8}$<br>$t_{CSSDS8}$<br>$t_{CSHS8}$ | CS1/CS0 | Chip select setup time | | 10<br>10<br>20 | | nS |

($1.8V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{ASS8}$ | CD | Address setup time | | 0 | – | nS |
| $t_{AHS8}$ | | Address hold time | | 60 | – | nS |
| $t_{CYS8}$ | SCK | System cycle time | | 200 | – | nS |
| $t_{LPWS8}$ | | Low pulse width | | 95 | – | nS |
| $t_{HPWS8}$ | | High pulse width | | 95 | – | nS |
| $t_{DSS8}$<br>$t_{DHS8}$ | SDA | Data setup time<br>Data hold time | | 30<br>25 | – | nS |
| $t_{CSSAS8}$<br>$t_{CSSDS8}$<br>$t_{CSHS8}$ | CS1/CS0 | Chip select setup time | | 10<br>10<br>20 | | nS |

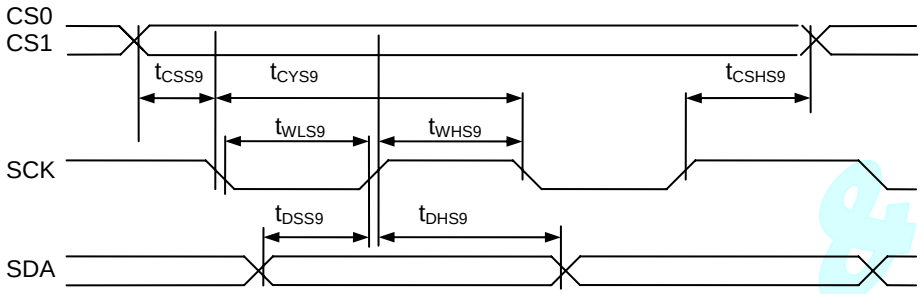



**FIGURE 13:** Serial Bus Timing Characteristics (for S9)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{CYS9}$ | SCK | System cycle time | | 80 | – | nS |
| $t_{LPWS9}$ | | Low pulse width | | 35 | – | nS |
| $t_{HPWS9}$ | | High pulse width | | 35 | – | nS |
| $t_{DSS9}$<br>$t_{DHS9}$ | SDA | Data setup time<br>Data hold time | | 30<br>20 | – | nS |
| $t_{CSSAS9}$<br>$t_{CSHS9}$ | CS1/CS0 | Chip select setup time | | 5<br>5 | | nS |

($1.8V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{CYS9}$ | SCK | System cycle time | | 160 | – | nS |
| $t_{LPWS9}$ | | Low pulse width | | 70 | – | nS |
| $t_{HPWS9}$ | | High pulse width | | 70 | – | nS |
| $t_{DSS9}$<br>$t_{DHS9}$ | SDA | Data setup time<br>Data hold time | | 60<br>40 | – | nS |
| $t_{CSSAS9}$<br>$t_{CSHS9}$ | CS1/CS0 | Chip select setup time | | 10<br>10 | | nS |

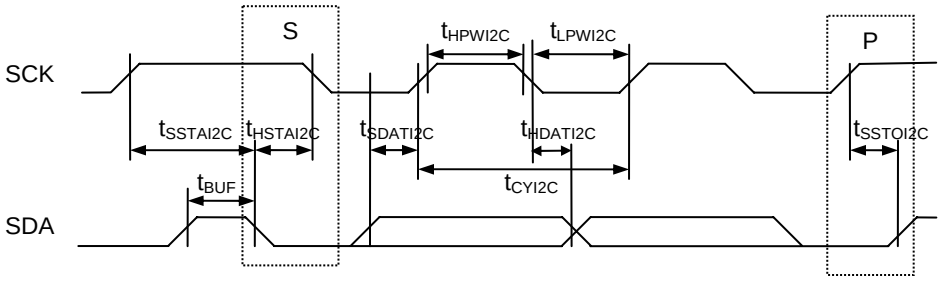



**FIGURE 14** Serial bus timing characteristics (for $I^2C$)

(2.5V ⩽ $V_{DD}$ < 3.3V, Ta= –30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{CYI2C}$ | SCK | SCK cycle time | tr+tf ⩽ 100nS | 250 | – | nS |
| $t_{LPWI2C}$ | | Low pulse width | | 65 | – | nS |
| $t_{HPWI2C}$ | | High pulse width | | 65 | – | nS |
| tr, tf | SCK SDA | Rise time and fall time | | – | – | nS |
| $t_{SSDAI2C}$ | | Data setup time | | 25 | – | nS |
| $t_{HDAI2C}$ | | Data hold time | | 10 | – | nS |
| $t_{SSTAI2C}$ | | START Setup time | | 25 | – | nS |
| $t_{HSTAI2C}$ | | START Hold time | | 20 | – | nS |
| $t_{SSTOI2C}$ | | STOP setup time | | 25 | – | nS |

(1.8V ⩽ $V_{DD}$ < 2.5V, Ta= –30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{CYI2C}$ | SCK | SCK cycle time | tr+tf ⩽ 100nS | 300 | – | nS |
| $t_{LPWI2C}$ | | Low pulse width | | 100 | – | nS |
| $t_{HPWI2C}$ | | High pulse width | | 100 | – | nS |
| tr, tf | SCK SDA | Rise time and fall time | | – | – | nS |
| $t_{SSDAI2C}$ | | Data setup time | | 40 | – | nS |
| $t_{HDAI2C}$ | | Data hold time | | 10 | – | nS |
| $t_{SSTAI2C}$ | | START Setup time | | 25 | – | nS |
| $t_{HSTAI2C}$ | | START Hold time | | 35 | – | nS |
| $t_{SSTOI2C}$ | | STOP setup time | | 25 | – | nS |

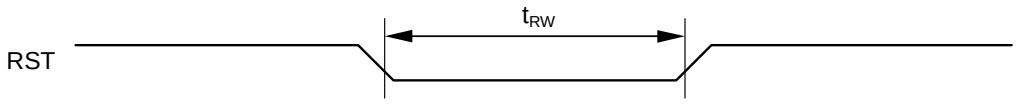



**FIGURE 15:** Reset Characteristics

(1.8V ≤ $V_{DD}$ < 3.3V, Ta= –30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{RW}$ | RST | Reset low pulse width | | 1 | – | µS |

## PHYSICAL DIMENSIONS

**DIE SIZE:**
5600x910 μM$^2$

**DIE THICKNESS:**
0.4 mm

**BUMP HEIGHT:**
15 μM (within die)
($H_{MAX}$ – $H_{MIN}$) within die < 2 μM

**COM/SEG SIZE:**
29x76 μM (Typ.)

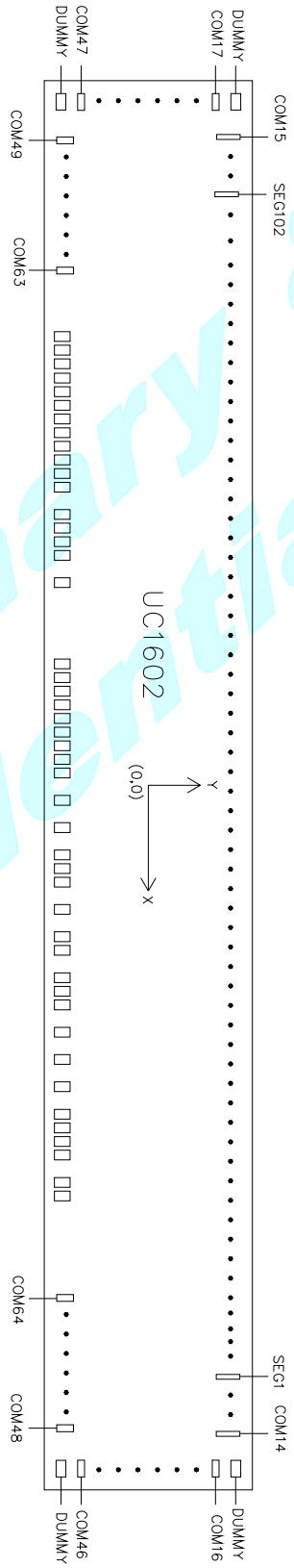
**BUMP PITCH:**
COM : 44 μM (Typ.)
SEG : 44 μM (Typ.)

**BUMP GAP:**
15 μM (MIN.)

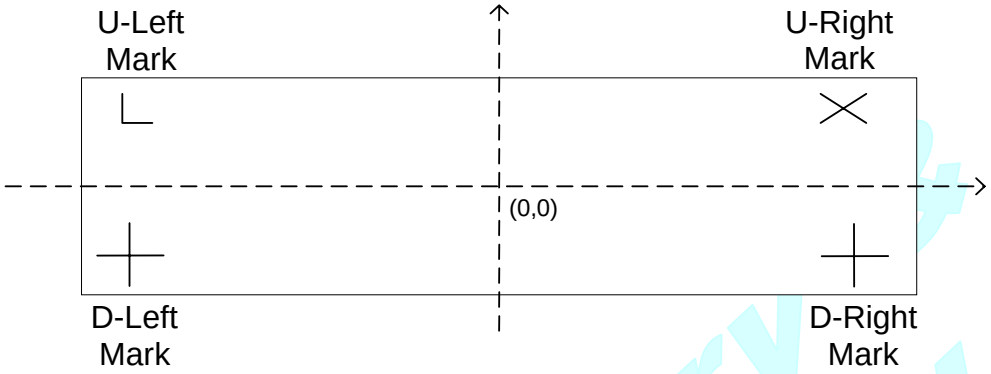
**COORDINATE ORIGIN:**
Chip center

**PAD REFERENCE:**
Pad center

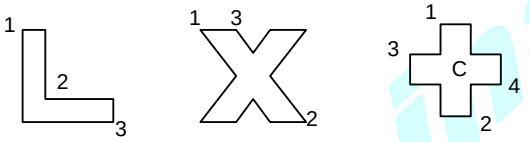
(Drawing and coordinates are for the Circuit/Bump view.)



## ALIGNMENT MARK INFORMATION




**SHAPE OF THE ALIGNMENT MARK:**




**NOTE:**

Alignment mark is on Metal3 under Passivation.

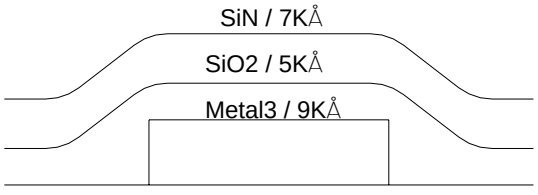
**COORDINATES:**

| | U-Left Mark | | U-Right Mark | |
|---|---|---|---|---|
| | X | Y | X | Y |
| 1 | -2662.5 | 376.5 | 2622.5 | 376.5 |
| 2 | -2646.9 | 352.0 | 2662.5 | 336.5 |
| 3 | -2622.5 | 336.5 | 2632.5 | 376.5 |

| | D-Left Mark Center | | D-Right Mark Center | |
|---|---|---|---|---|
| | X | Y | X | Y |
| 1 | -2632.0 | -308.0 | 2612.0 | -308.0 |
| 2 | -2612.0 | -373.0 | 2632.0 | -373.0 |
| 3 | -2654.5 | -330.5 | 2589.5 | -330.5 |
| 4 | -2589.5 | -350.5 | 2654.5 | -350.5 |
| C | -2622.0 | -340.5 | 2622.0 | -340.5 |

(The values of the x-coordinate and the y-coordinate in the table are after rounded.)

**TOP METAL AND PASSIVATION:**




**FOR NON-OTP PROCESS CROSS-SECTION**

## PAD COORDINATES

| # | Pad | X | Y | W | H |
|---|---|---|---|---|---|
| 1 | DUMMY | -2712 | 380 | 76 | 41 |
| 2 | COM17 | -2712 | 330 | 76 | 29 |
| 3 | COM19 | -2712 | 286 | 76 | 29 |
| 4 | COM21 | -2712 | 242 | 76 | 29 |
| 5 | COM23 | -2712 | 198 | 76 | 29 |
| 6 | COM25 | -2712 | 154 | 76 | 29 |
| 7 | COM27 | -2712 | 110 | 76 | 29 |
| 8 | COM29 | -2712 | 66 | 76 | 29 |
| 9 | COM31 | -2712 | 22 | 76 | 29 |
| 10 | COM33 | -2712 | -22 | 76 | 29 |
| 11 | COM35 | -2712 | -66 | 76 | 29 |
| 12 | COM37 | -2712 | -110 | 76 | 29 |
| 13 | COM39 | -2712 | -154 | 76 | 29 |
| 14 | COM41 | -2712 | -198 | 76 | 29 |
| 15 | COM43 | -2712 | -242 | 76 | 29 |
| 16 | COM45 | -2712 | -286 | 76 | 29 |
| 17 | COM47 | -2712 | -330 | 76 | 29 |
| 18 | DUMMY | -2712 | -380 | 76 | 41 |
| 19 | COM49 | -2534.5 | -367 | 29 | 76 |
| 20 | COM51 | -2490.5 | -367 | 29 | 76 |
| 21 | COM53 | -2446.5 | -367 | 29 | 76 |
| 22 | COM55 | -2402.5 | -367 | 29 | 76 |
| 23 | COM57 | -2358.5 | -367 | 29 | 76 |
| 24 | COM59 | -2314.5 | -367 | 29 | 76 |
| 25 | COM61 | -2270.5 | -367 | 29 | 76 |
| 26 | COM63 | -2226.5 | -367 | 29 | 76 |
| 27 | RIC | -2182.5 | -367 | 29 | 76 |
| 28 | CS0 | -2031.6 | -363 | 42 | 82 |
| 29 | VDDX | -1971.6 | -363 | 42 | 82 |
| 30 | CS1 | -1911.6 | -363 | 42 | 82 |
| 31 | TST4 | -1840.6 | -363 | 42 | 82 |
| 32 | RST_ | -1756.6 | -363 | 42 | 82 |
| 33 | CD | -1672.6 | -363 | 42 | 82 |
| 34 | D0 | -1612.6 | -363 | 42 | 82 |
| 35 | D1 | -1369.6 | -363 | 42 | 82 |
| 36 | VDD | -1309.6 | -363 | 42 | 82 |
| 37 | VDD2 | -859.2 | -363 | 42 | 82 |
| 38 | VDD3 | -597.4 | -363 | 42 | 82 |
| 39 | VSS2 | -427.4 | -363 | 42 | 82 |
| 40 | VSS2 | -367.4 | -363 | 42 | 82 |
| 41 | VSS | -197.4 | -363 | 42 | 82 |
| 42 | VSS | -137.4 | -363 | 42 | 82 |
| 43 | TST2 | 25.2 | -363 | 42 | 82 |
| 44 | VB1+ | 85.2 | -363 | 42 | 82 |
| 45 | VB1+ | 145.2 | -363 | 42 | 82 |
| 46 | BM0 | 452.2 | -363 | 42 | 82 |
| 47 | VDDX | 512.2 | -363 | 42 | 82 |
| 48 | BM1 | 572.2 | -363 | 42 | 82 |
| 49 | VB1- | 879.2 | -363 | 42 | 82 |
| 50 | VB1- | 939.2 | -363 | 42 | 82 |
| 51 | VB0- | 999.2 | -363 | 42 | 82 |
| 52 | VB0- | 1059.2 | -363 | 42 | 82 |
| 53 | VB0+ | 1416.2 | -363 | 42 | 82 |
| 54 | VB0+ | 1476.2 | -363 | 42 | 82 |

| # | Pad | X | Y | W | H |
|---|---|---|---|---|---|
| 55 | VLCDOUT | 1536.2 | -363 | 42 | 82 |
| 56 | VLCDIN | 1964.2 | -363 | 42 | 82 |
| 57 | VDD2 | 2024.2 | -363 | 42 | 82 |
| 58 | COM64 | 2182.5 | -367 | 29 | 76 |
| 59 | COM62 | 2226.5 | -367 | 29 | 76 |
| 60 | COM60 | 2270.5 | -367 | 29 | 76 |
| 61 | COM58 | 2314.5 | -367 | 29 | 76 |
| 62 | COM56 | 2358.5 | -367 | 29 | 76 |
| 63 | COM54 | 2402.5 | -367 | 29 | 76 |
| 64 | COM52 | 2446.5 | -367 | 29 | 76 |
| 65 | COM50 | 2490.5 | -367 | 29 | 76 |
| 66 | COM48 | 2534.5 | -367 | 29 | 76 |
| 67 | DUMMY | 2712 | -380 | 76 | 41 |
| 68 | COM46 | 2712 | -330 | 76 | 29 |
| 69 | COM44 | 2712 | -286 | 76 | 29 |
| 70 | COM42 | 2712 | -242 | 76 | 29 |
| 71 | COM40 | 2712 | -198 | 76 | 29 |
| 72 | COM38 | 2712 | -154 | 76 | 29 |
| 73 | COM36 | 2712 | -110 | 76 | 29 |
| 74 | COM34 | 2712 | -66 | 76 | 29 |
| 75 | COM32 | 2712 | -22 | 76 | 29 |
| 76 | COM30 | 2712 | 22 | 76 | 29 |
| 77 | COM28 | 2712 | 66 | 76 | 29 |
| 78 | COM26 | 2712 | 110 | 76 | 29 |
| 79 | COM24 | 2712 | 154 | 76 | 29 |
| 80 | COM22 | 2712 | 198 | 76 | 29 |
| 81 | COM20 | 2712 | 242 | 76 | 29 |
| 82 | COM18 | 2712 | 286 | 76 | 29 |
| 83 | COM16 | 2712 | 330 | 76 | 29 |
| 84 | DUMMY | 2712 | 380 | 76 | 41 |
| 85 | COM14 | 2574 | 367 | 29 | 76 |
| 86 | COM12 | 2530 | 367 | 29 | 76 |
| 87 | COM10 | 2486 | 367 | 29 | 76 |
| 88 | COM8 | 2442 | 367 | 29 | 76 |
| 89 | COM6 | 2398 | 367 | 29 | 76 |
| 90 | COM4 | 2354 | 367 | 29 | 76 |
| 91 | COM2 | 2310 | 367 | 29 | 76 |
| 92 | RIC | 2266 | 367 | 29 | 76 |
| 93 | SEG1 | 2222 | 367 | 29 | 76 |
| 94 | SEG2 | 2178 | 367 | 29 | 76 |
| 95 | SEG3 | 2134 | 367 | 29 | 76 |
| 96 | SEG4 | 2090 | 367 | 29 | 76 |
| 97 | SEG5 | 2046 | 367 | 29 | 76 |
| 98 | SEG6 | 2002 | 367 | 29 | 76 |
| 99 | SEG7 | 1958 | 367 | 29 | 76 |
| 100 | SEG8 | 1914 | 367 | 29 | 76 |
| 101 | SEG9 | 1870 | 367 | 29 | 76 |
| 102 | SEG10 | 1826 | 367 | 29 | 76 |
| 103 | SEG11 | 1782 | 367 | 29 | 76 |
| 104 | SEG12 | 1738 | 367 | 29 | 76 |
| 105 | SEG13 | 1694 | 367 | 29 | 76 |
| 106 | SEG14 | 1650 | 367 | 29 | 76 |
| 107 | SEG15 | 1606 | 367 | 29 | 76 |
| 108 | SEG16 | 1562 | 367 | 29 | 76 |

| # | Pad | X | Y | W | H |
|---|---|---|---|---|---|
| 109 | SEG17 | 1518 | 367 | 29 | 76 |
| 110 | SEG18 | 1474 | 367 | 29 | 76 |
| 111 | SEG19 | 1430 | 367 | 29 | 76 |
| 112 | SEG20 | 1386 | 367 | 29 | 76 |
| 113 | SEG21 | 1342 | 367 | 29 | 76 |
| 114 | SEG22 | 1298 | 367 | 29 | 76 |
| 115 | SEG23 | 1254 | 367 | 29 | 76 |
| 116 | SEG24 | 1210 | 367 | 29 | 76 |
| 117 | SEG25 | 1166 | 367 | 29 | 76 |
| 118 | SEG26 | 1122 | 367 | 29 | 76 |
| 119 | SEG27 | 1078 | 367 | 29 | 76 |
| 120 | SEG28 | 1034 | 367 | 29 | 76 |
| 121 | SEG29 | 990 | 367 | 29 | 76 |
| 122 | SEG30 | 946 | 367 | 29 | 76 |
| 123 | SEG31 | 902 | 367 | 29 | 76 |
| 124 | SEG32 | 858 | 367 | 29 | 76 |
| 125 | SEG33 | 814 | 367 | 29 | 76 |
| 126 | SEG34 | 770 | 367 | 29 | 76 |
| 127 | SEG35 | 726 | 367 | 29 | 76 |
| 128 | SEG36 | 682 | 367 | 29 | 76 |
| 129 | SEG37 | 638 | 367 | 29 | 76 |
| 130 | SEG38 | 594 | 367 | 29 | 76 |
| 131 | SEG39 | 550 | 367 | 29 | 76 |
| 132 | SEG40 | 506 | 367 | 29 | 76 |
| 133 | SEG41 | 462 | 367 | 29 | 76 |
| 134 | SEG42 | 418 | 367 | 29 | 76 |
| 135 | SEG43 | 374 | 367 | 29 | 76 |
| 136 | SEG44 | 330 | 367 | 29 | 76 |
| 137 | SEG45 | 286 | 367 | 29 | 76 |
| 138 | SEG46 | 242 | 367 | 29 | 76 |
| 139 | SEG47 | 198 | 367 | 29 | 76 |
| 140 | SEG48 | 154 | 367 | 29 | 76 |
| 141 | SEG49 | 110 | 367 | 29 | 76 |
| 142 | SEG50 | 66 | 367 | 29 | 76 |
| 143 | SEG51 | 22 | 367 | 29 | 76 |
| 144 | SEG52 | -22 | 367 | 29 | 76 |
| 145 | SEG53 | -66 | 367 | 29 | 76 |
| 146 | SEG54 | -110 | 367 | 29 | 76 |
| 147 | SEG55 | -154 | 367 | 29 | 76 |
| 148 | SEG56 | -198 | 367 | 29 | 76 |
| 149 | SEG57 | -242 | 367 | 29 | 76 |
| 150 | SEG58 | -286 | 367 | 29 | 76 |
| 151 | SEG59 | -330 | 367 | 29 | 76 |
| 152 | SEG60 | -374 | 367 | 29 | 76 |
| 153 | SEG61 | -418 | 367 | 29 | 76 |
| 154 | SEG62 | -462 | 367 | 29 | 76 |
| 155 | SEG63 | -506 | 367 | 29 | 76 |
| 156 | SEG64 | -550 | 367 | 29 | 76 |
| 157 | SEG65 | -594 | 367 | 29 | 76 |
| 158 | SEG66 | -638 | 367 | 29 | 76 |
| 159 | SEG67 | -682 | 367 | 29 | 76 |
| 160 | SEG68 | -726 | 367 | 29 | 76 |
| 161 | SEG69 | -770 | 367 | 29 | 76 |
| 162 | SEG70 | -814 | 367 | 29 | 76 |
| 163 | SEG71 | -858 | 367 | 29 | 76 |

| # | Pad | X | Y | W | H |
|---|---|---|---|---|---|
| 164 | SEG72 | -902 | 367 | 29 | 76 |
| 165 | SEG73 | -946 | 367 | 29 | 76 |
| 166 | SEG74 | -990 | 367 | 29 | 76 |
| 167 | SEG75 | -1034 | 367 | 29 | 76 |
| 168 | SEG76 | -1078 | 367 | 29 | 76 |
| 169 | SEG77 | -1122 | 367 | 29 | 76 |
| 170 | SEG78 | -1166 | 367 | 29 | 76 |
| 171 | SEG79 | -1210 | 367 | 29 | 76 |
| 172 | SEG80 | -1254 | 367 | 29 | 76 |
| 173 | SEG81 | -1298 | 367 | 29 | 76 |
| 174 | SEG82 | -1342 | 367 | 29 | 76 |
| 175 | SEG83 | -1386 | 367 | 29 | 76 |
| 176 | SEG84 | -1430 | 367 | 29 | 76 |
| 177 | SEG85 | -1474 | 367 | 29 | 76 |
| 178 | SEG86 | -1518 | 367 | 29 | 76 |
| 179 | SEG87 | -1562 | 367 | 29 | 76 |
| 180 | SEG88 | -1606 | 367 | 29 | 76 |
| 181 | SEG89 | -1650 | 367 | 29 | 76 |
| 182 | SEG90 | -1694 | 367 | 29 | 76 |
| 183 | SEG91 | -1738 | 367 | 29 | 76 |
| 184 | SEG92 | -1782 | 367 | 29 | 76 |
| 185 | SEG93 | -1826 | 367 | 29 | 76 |
| 186 | SEG94 | -1870 | 367 | 29 | 76 |
| 187 | SEG95 | -1914 | 367 | 29 | 76 |
| 188 | SEG96 | -1958 | 367 | 29 | 76 |
| 189 | SEG97 | -2002 | 367 | 29 | 76 |
| 190 | SEG98 | -2046 | 367 | 29 | 76 |
| 191 | SEG99 | -2090 | 367 | 29 | 76 |
| 192 | SEG100 | -2134 | 367 | 29 | 76 |
| 193 | SEG101 | -2178 | 367 | 29 | 76 |
| 194 | SEG102 | -2222 | 367 | 29 | 76 |
| 195 | COM1 | -2266 | 367 | 29 | 76 |
| 196 | COM3 | -2310 | 367 | 29 | 76 |
| 197 | COM5 | -2354 | 367 | 29 | 76 |
| 198 | COM7 | -2398 | 367 | 29 | 76 |
| 199 | COM9 | -2442 | 367 | 29 | 76 |
| 200 | COM11 | -2486 | 367 | 29 | 76 |
| 201 | COM13 | -2530 | 367 | 29 | 76 |
| 202 | COM15 | -2574 | 367 | 29 | 76 |

(The values of the x-coordinate and the y-coordinate in the table are after-rounded.)

## TRAY INFORMATION

(TBD)