

Preliminary W29C011A



128K × 8 CMOS FLASH MEMORY

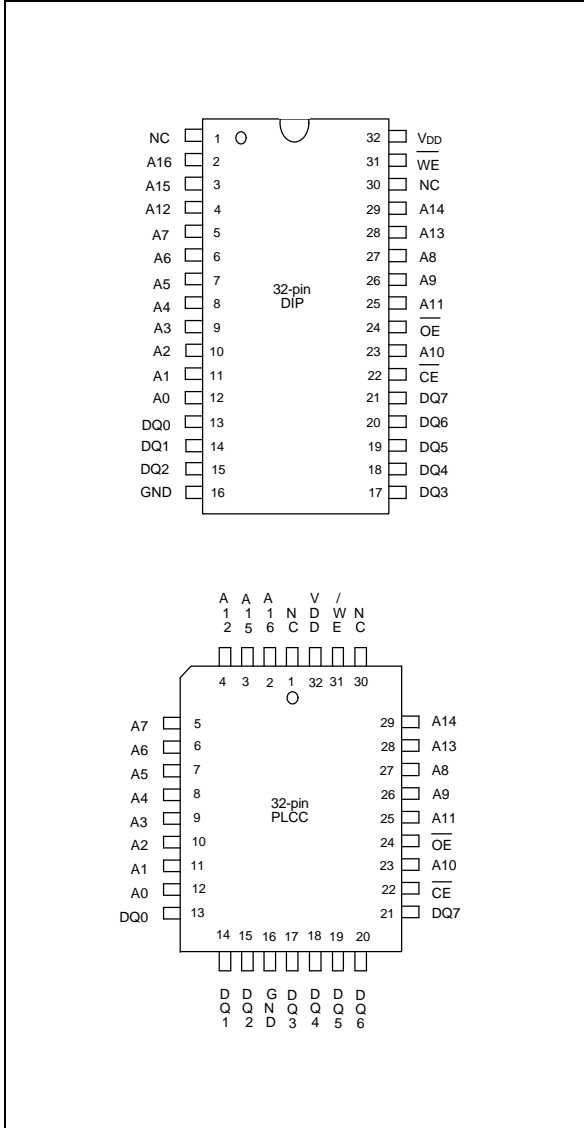
GENERAL DESCRIPTION

The W29C011A is a 1-megabit, 5-volt only CMOS flash memory organized as 128K × 8 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W29C011A results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

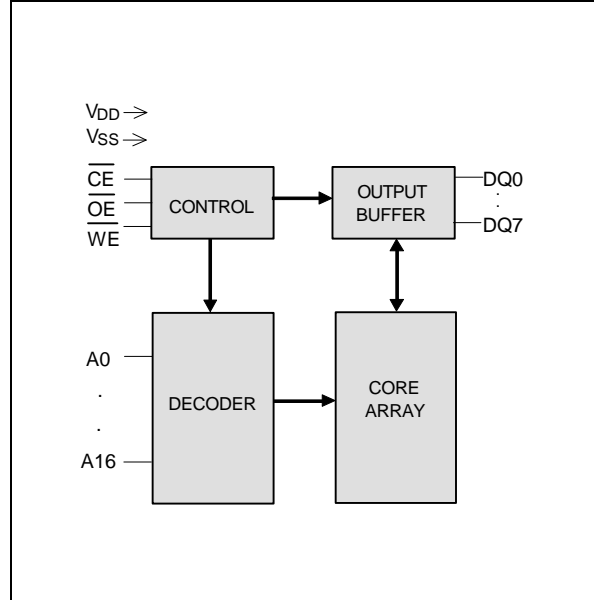
FEATURES

- Single 5-volt program and erase operations
- Fast page-write operations
 - 128 bytes per page
 - Page program cycle: 10 mS (max.)
 - Effective byte-program cycle time: 39 μS
 - Software-protected data write
- Fast chip-erase operation: 50 mS
- Read access time: 150 nS
- Page program/erase cycles: 1,000
- Ten-year data retention
- Software and hardware data protection
- Low power consumption
 - Active current: 25 mA (typ.)
 - Standby current: 20 μA (typ.)
- Automatic program timing with internal V_{PP} generation
- End of program detection
 - Toggle bit
 - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin 600 mil DIP, 450 mil SOP and PLCC

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A16	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
\overline{WE}	Write Enable
V _{DD}	Power Supply
GND	Ground
NC	No Connection



FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W29C011A is controlled by \overline{CE} and \overline{OE} , both of which have to be low for the host to obtain data from the outputs. \overline{CE} is used for device selection. When \overline{CE} is high, the chip is de-selected and only standby power will be consumed. \overline{OE} is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either \overline{CE} or \overline{OE} is high. Refer to the timing waveforms for further details.

Page Write Mode

The W29C011A is programmed on a page basis. Every page contains 128 bytes of data. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded will be erased to "FFh" during programming of the page.

The write operation is initiated by forcing \overline{CE} and \overline{WE} low and \overline{OE} high. The write procedure consists of two steps. Step 1 is the byte-load cycle, in which the host writes to the page buffer of the device. Step 2 is an internal programming cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the byte-load cycle, the addresses are latched by the falling edge of either \overline{CE} or \overline{WE} , whichever occurs last. The data are latched by the rising edge of either \overline{CE} or \overline{WE} , whichever occurs first. If the host loads a second byte into the page buffer within a byte-load cycle time (TBLC) of 200 μ S, after the initial byte-load cycle, the W29C011A will stay in the page load cycle. Additional bytes can then be loaded consecutively. The page load cycle will be terminated and the internal programming cycle will start if no additional byte is loaded into the page buffer within 300 μ S (TBLCO) from the last byte-load cycle, i.e., there is no subsequent \overline{WE} high-to-low transition after the last rising edge of \overline{WE} . A7 to A16 specify the page address. All bytes that are loaded into the page buffer must have the same page address. A0 to A6 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

In the internal programming cycle, all data in the page buffers, i.e., 128 bytes of data, are written simultaneously into the memory array. Before the completion of the internal programming cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

Software-protected Data Write

The device provides a JEDEC-approved software-protected data write. Once this scheme is enabled, any write operation requires a series of three-byte program commands (with specific data to a specific address) to be performed before the data load operation. The three-byte load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29C011A is shipped with the software data protection enabled. To enable the software data protection scheme, perform the three-byte command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-byte program command cycle.



Hardware Data Protection

The integrity of the data stored in the W29C011A is also hardware protected in the following ways:

- (1) Noise/Glitch Protection: A \overline{WE} pulse of less than 15 nS in duration will not initiate a write cycle.
- (2) V_{DD} Power Up/Down Detection: The programming operation is inhibited when V_{DD} is less than 3.8V.
- (3) Write Inhibit Mode: Forcing \overline{OE} low, \overline{CE} high, or \overline{WE} high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

Data Polling (DQ7)-Write Status Detection

The W29C011A includes a data polling feature to indicate the end of a programming cycle. When the W29C011A is in the internal programming cycle, any attempt to read DQ7 of the last byte loaded during the page/byte-load cycle will receive the complement of the true data. Once the programming cycle is completed, DQ7 will show the true data.

Toggle Bit (DQ6)-Write Status Detection

In addition to data polling, the W29C011A provides another method for determining the end of a program cycle. During the internal programming cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the programming cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

5-Volt-Only Software Chip Erase

The chip-erase mode can be initiated by a six-byte command sequence. After the command loading cycles, the device enters the internal chip erase mode, which is automatically timed and will be completed in 50 mS. The host system is not required to provide any control or timing during this operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-byte command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (DAh). A read from address 0001H outputs the device code (C1h). The product ID operation can be terminated by a three-byte command sequence.

In the hardware access mode, access to the product ID is activated by forcing \overline{CE} and \overline{OE} low, \overline{WE} high, and raising A9 to 12 volts.



TABLE OF OPERATING MODES

Operating Mode Selection

Operating Range = 0 to 70°C (Ambient Temperature), VDD = 5V ±10%, VSS = 0V, VIH = 12V

MODE	PINS				
	\overline{CE}	\overline{OE}	\overline{WE}	ADDRESS	DQ.
Read	VIL	VIL	VIH	A1N	Dout
Write	VIL	VIH	VIL	A1N	Din
Standby	VIH	X	X	X	High Z
Write Inhibit	X	VIL	X	X	High Z/DOUT
	X	X	VIH	X	High Z/DOUT
Output Disable	X	VIH	X	X	High Z
5-Volt Software Chip Erase	VIL	VIH	VIL	A1N	DIN
Product ID	VIL	VIL	VIH	A0 = VIL; A1-A16 = VIL; A9 = VIH	Manufacturer Code DA (Hex)
	VIL	VIL	VIH	A0 = VIH; A1-A16 = VIL; A9 = VIH	Device Code C1 (Hex)

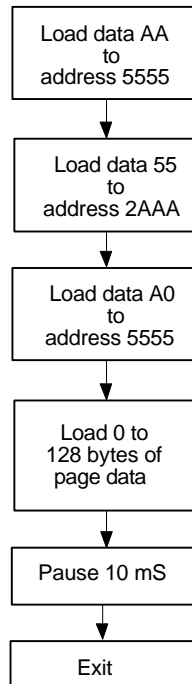


Command Codes for Software Data Protection Write

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	A0H

Software Data Protection Acquisition Flow

Software Data Protection Write Flow



Notes for software program code:

Data Format: DQ7–DQ0 (Hex)

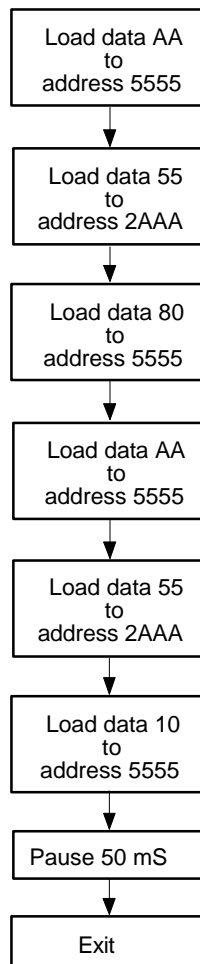
Address Format: A14–A0 (Hex)



Command Codes for Software Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	80H
3 Write	5555H	AAH
4 Write	2AAAH	55H
5 Write	5555H	10H

Software Chip Erase Acquisition Flow



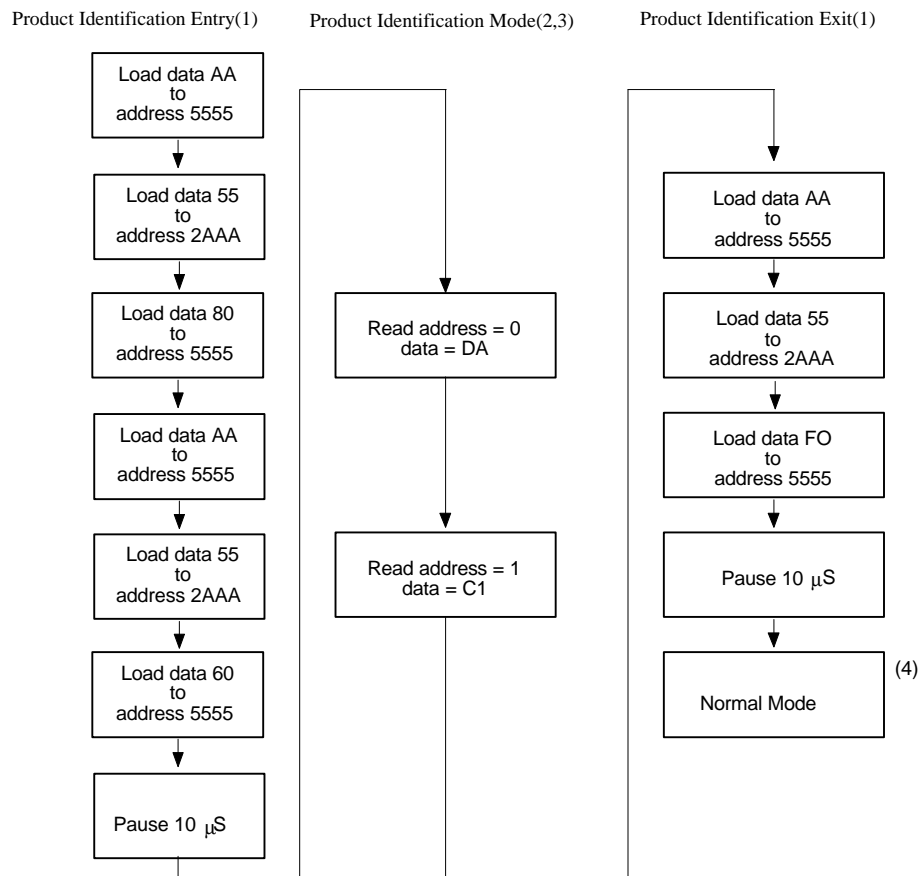
Notes for software chip erase:
 Data Format: DQ7–DQ0 (Hex)
 Address Format: A14–A0 (Hex)



Command Codes for Product Identification

BYTE SEQUENCE	SOFTWARE PRODUCT IDENTIFICATION ENTRY		SOFTWARE PRODUCT IDENTIFICATION EXIT	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	80H	5555H	F0H
3 Write	5555H	AAH	-	-
4 Write	2AAAH	55H	-	-
5 Write	5555H	60H	-	-
Pause 10 μ S			Pause 10 μ S	

Software Product Identification Acquisition Flow



Notes for software product identification:

- (1) Data format: DQ7–DQ0 (Hex); address format: A14–A0 (Hex).
- (2) A1–A16 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.
- (3) The device does not remain in identification mode if power down.
- (4) The device returns to standard operation mode.

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DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V _{SS} Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except \overline{OE}	-0.5 to V _{DD} +1.0	V
Transient Voltage ($t_r \leq 20$ nS) on Any Pin to Ground Potential	-1.0 to V _{DD} +1.0	V
Voltage on \overline{OE} Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I _{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/Os open Address inputs = V _{IL} /V _{IH} , at f = 5 MHz	-	-	50	mA
Standby V _{DD} Current (TTL input)	I _{SB1}	$\overline{CE} = V_{IH}$, all I/Os open Other inputs = V _{IL} /V _{IH}	-	2	3	mA
Standby V _{DD} Current (CMOS input)	I _{SB2}	$\overline{CE} = V_{DD} - 0.3V$, all I/Os open Other inputs = V _{DD} - 0.3V/GND	-	20	100	μA
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{DD}	-	-	1	μA
Output Leakage Current	I _{LO}	V _{IN} = GND to V _{DD}	-	-	10	μA
Input Low Voltage	V _{IL}	-	-0.3	-	0.8	V
Input High Voltage	V _{IH}	-	2.0	-	V _{DD} +0.5	V
Output Low Voltage	V _{OL}	I _{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V _{OH}	I _{OH} = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU.READ	100	μS
Power-up to Write Operation	TPU.WRITE	5	mS



CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	C _{I/O}	V _{I/O} = 0V	12	pF
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF

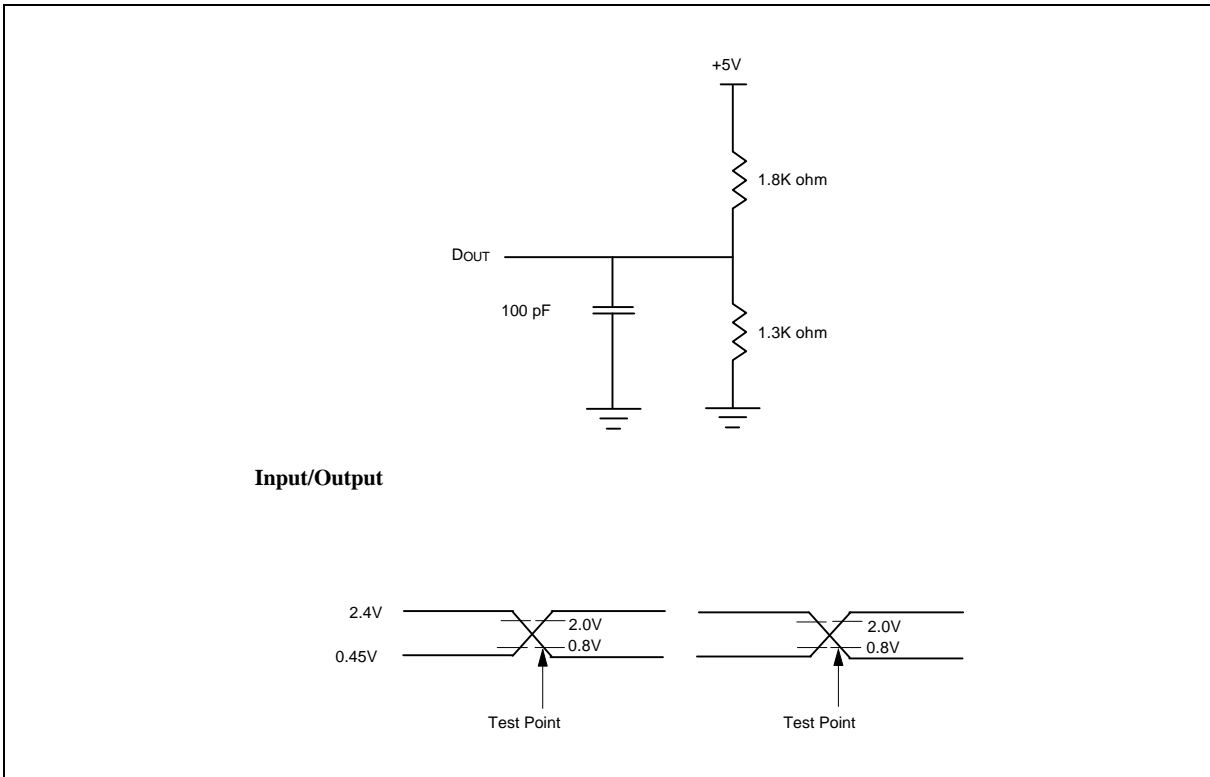
AC CHARACTERISTICS

AC Test Conditions

(V_{DD} = 5V ±10%)

PARAMETER	CONDITIONS
Input Pulse Levels	0.45V to 2.4V
Input Rise/Fall Time	10 nS
Input/Output Timing Level	0.8V/2.0V
Output Load	1 TTL Gate and C _L = 100 pF

AC Test Load and Waveforms



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Read Cycle Timing Parameters

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W29C011A-15		UNIT
		MIN.	MAX.	
Read Cycle Time	TRC	150	-	nS
Chip Enable Access Time	TCE	-	150	nS
Address Access Time	TAA	-	150	nS
Output Enable Access Time	TOE	-	70	nS
$\overline{\text{CE}}$ Low to Active Output	TCLZ	0	-	nS
$\overline{\text{OE}}$ Low to Active Output	TOLZ	0	-	nS
$\overline{\text{CE}}$ High to High-Z Output	TCHZ	-	45	nS
$\overline{\text{OE}}$ High to High-Z Output	TOHZ	-	45	nS
Output Hold from Address change	TOH	0	-	nS

Byte/Page-Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write Cycle (erase and program)	TWC	-	-	10	mS
Address Setup Time	TAS	0	-	-	nS
Address Hold Time	TAH	50	-	-	nS
$\overline{\text{WE}}$ and $\overline{\text{CE}}$ Setup Time	TCS	0	-	-	nS
$\overline{\text{WE}}$ and $\overline{\text{CE}}$ Hold Time	TCH	0	-	-	nS
$\overline{\text{OE}}$ High Setup Time	TOES	10	-	-	nS
$\overline{\text{OE}}$ High Hold Time	TOEH	10	-	-	nS
$\overline{\text{CE}}$ Pulse Width	TCP	70	-	-	nS
$\overline{\text{WE}}$ Pulse Width	TWP	70	-	-	nS
$\overline{\text{WE}}$ High Width	TWPH	150	-	-	nS
Data Setup Time	TDS	50	-	-	nS
Data Hold Time	TDH	10	-	-	nS
Byte Load Cycle Time	TBLC	0.22	-	200	μS
Byte Load Cycle Time-out	TBLCO	300	-	-	μS

Note: All AC timing signals observe the following guidelines for determining setup and hold times:

(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

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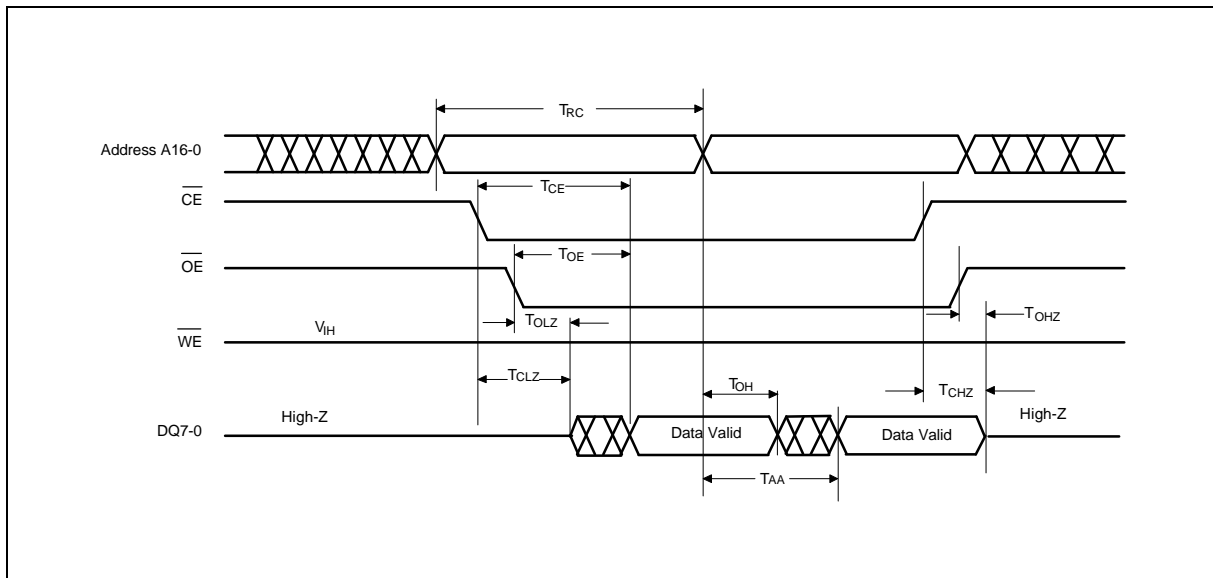


Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	W29C011A-15		UNIT
		MIN.	MAX.	
$\overline{\text{OE}}$ to Data Polling Output Delay	TOEP	-	70	nS
$\overline{\text{CE}}$ to Data Polling Output Delay	TCEP	-	150	nS
$\overline{\text{OE}}$ to Toggle Bit Output Delay	TOET	-	70	nS
$\overline{\text{CE}}$ to Toggle Bit Output Delay	TCET	-	150	nS

TIMING WAVEFORMS

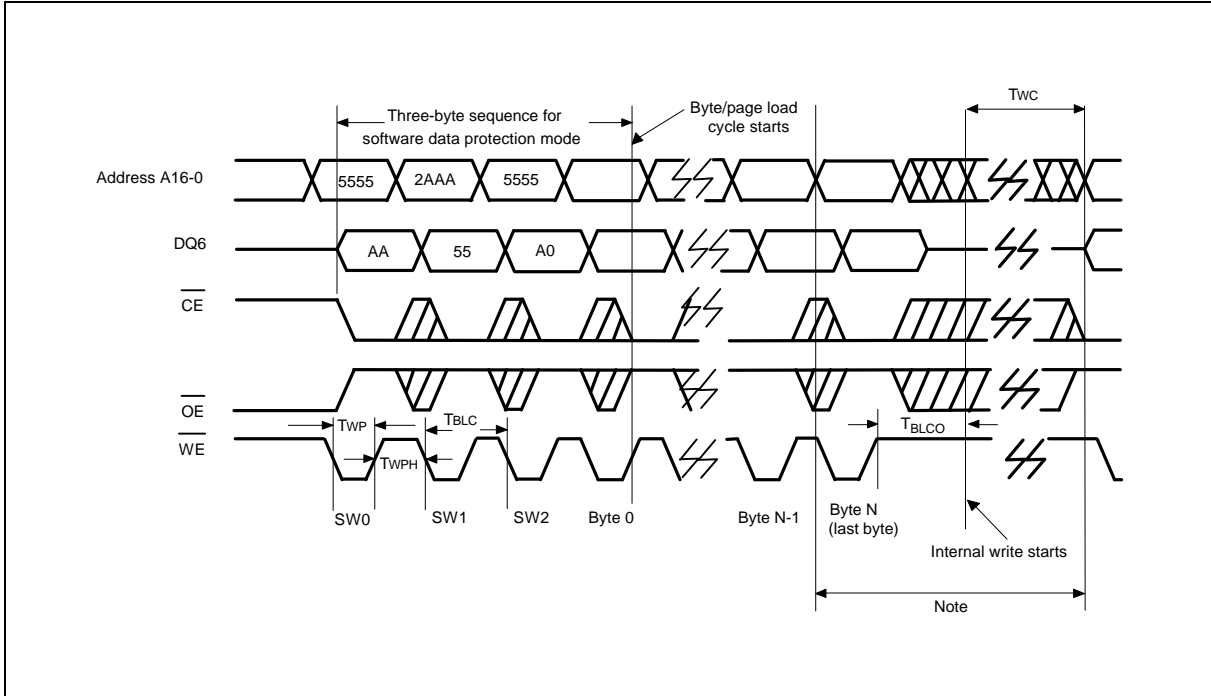
Read Cycle Timing Diagram





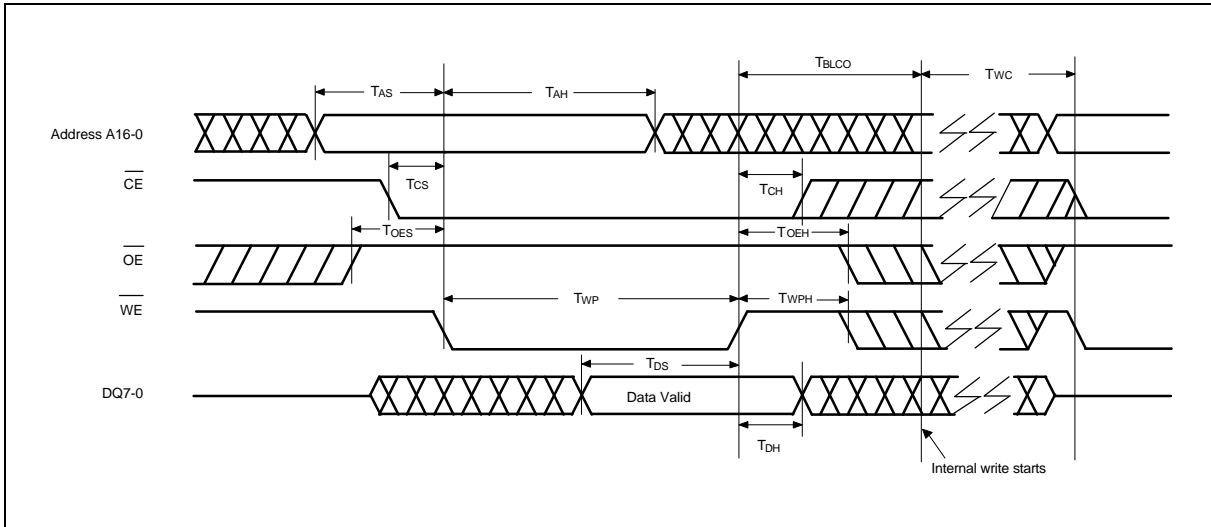
Timing Waveforms, continued

Page Write Timing Diagram



Notes: Refer to " $\overline{\text{CE}}$ ($\overline{\text{WE}}$) Controlled Write Cycle Timing Diagram" for a detailed timing diagram.

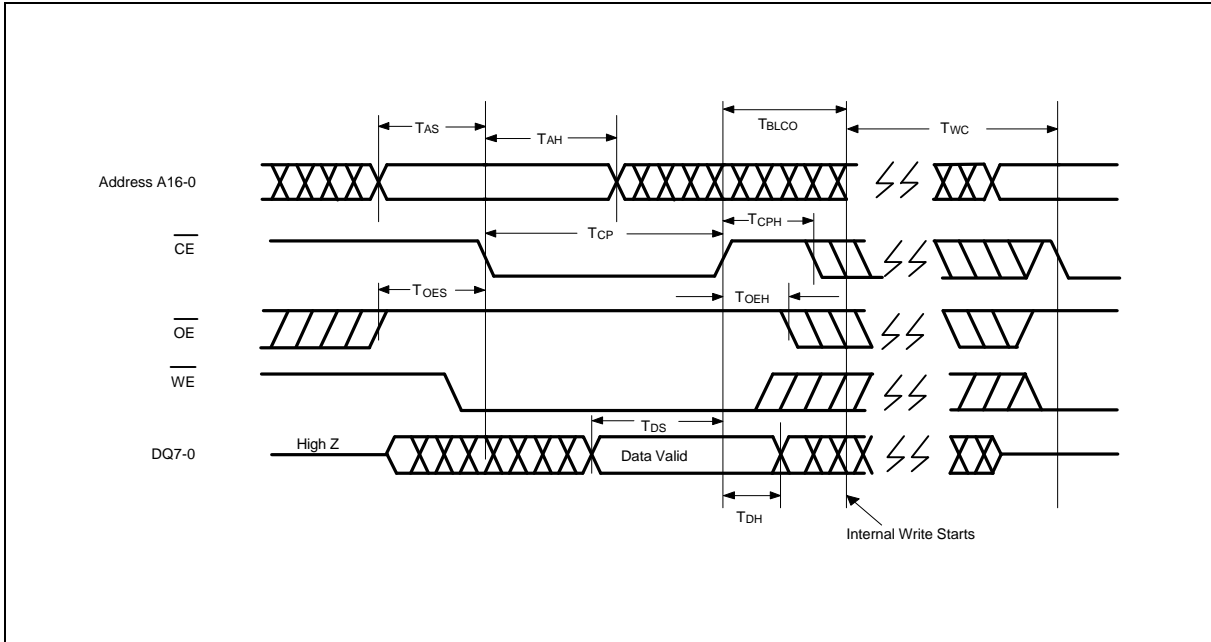
$\overline{\text{WE}}$ Controlled Write Cycle Timing Diagram



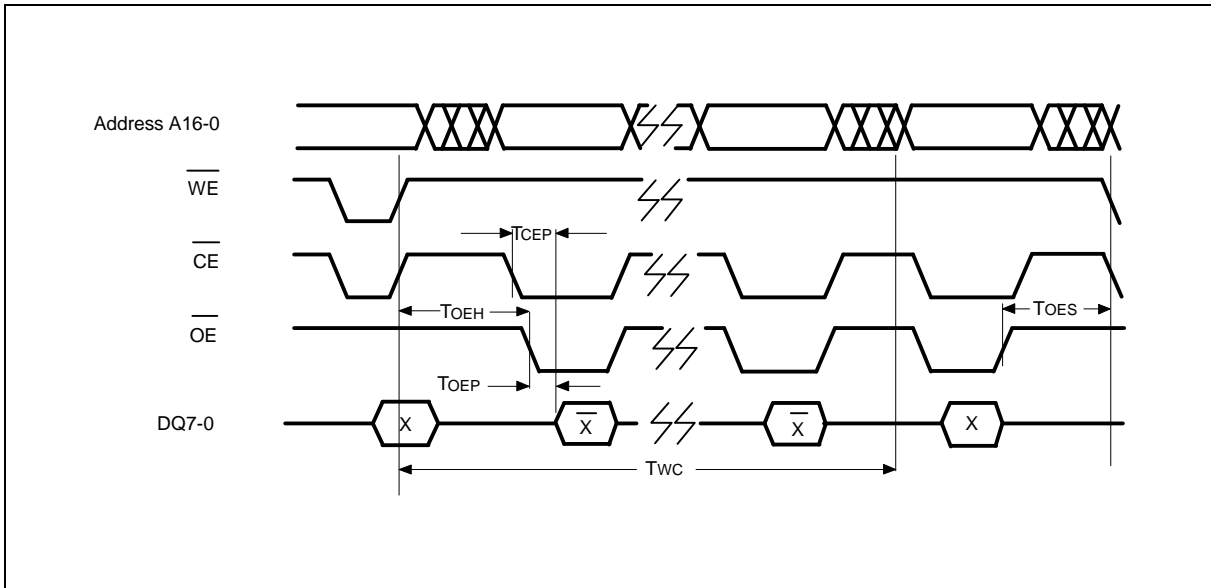


Timing Waveforms, continued

CE Controlled Write Cycle Timing Diagram



DATA Polling Timing Diagram

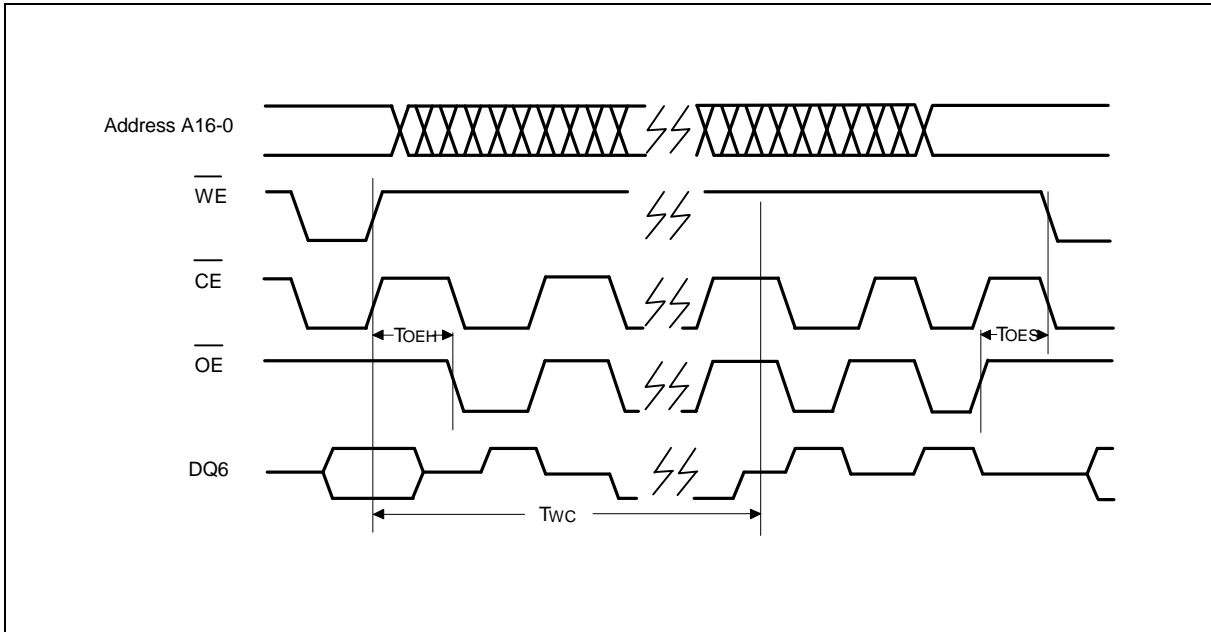


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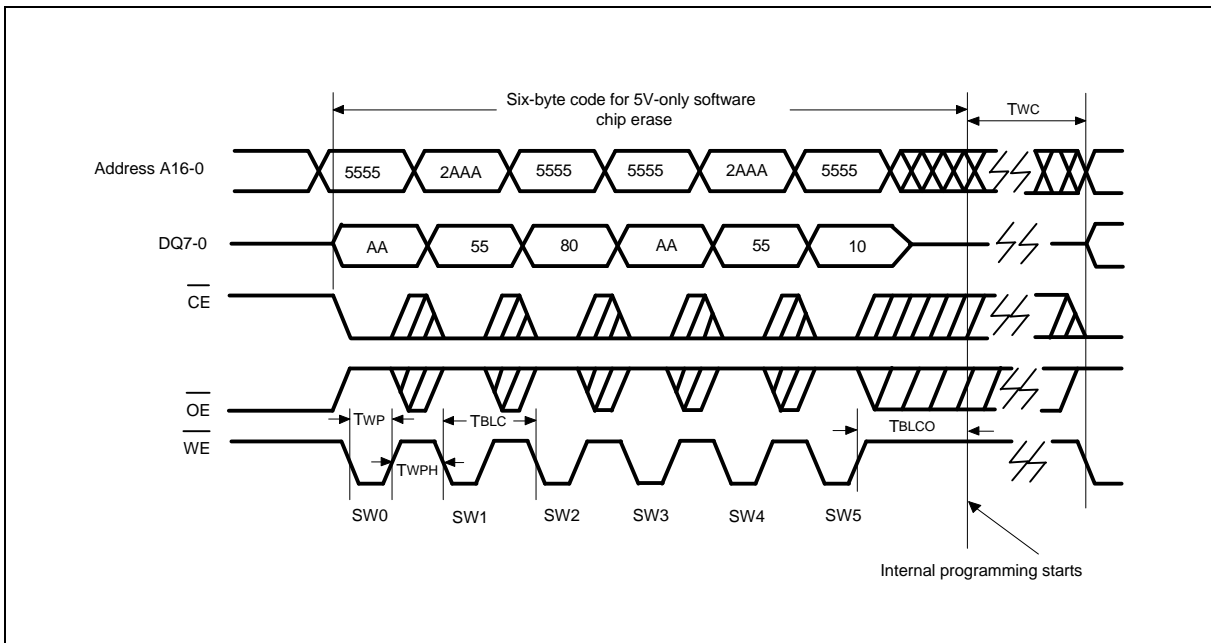


Timing Waveforms, continued

Toggle Bit Timing Diagram



5 Volt-Only Software Chip Erase Timing Diagram



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ORDERING INFORMATION

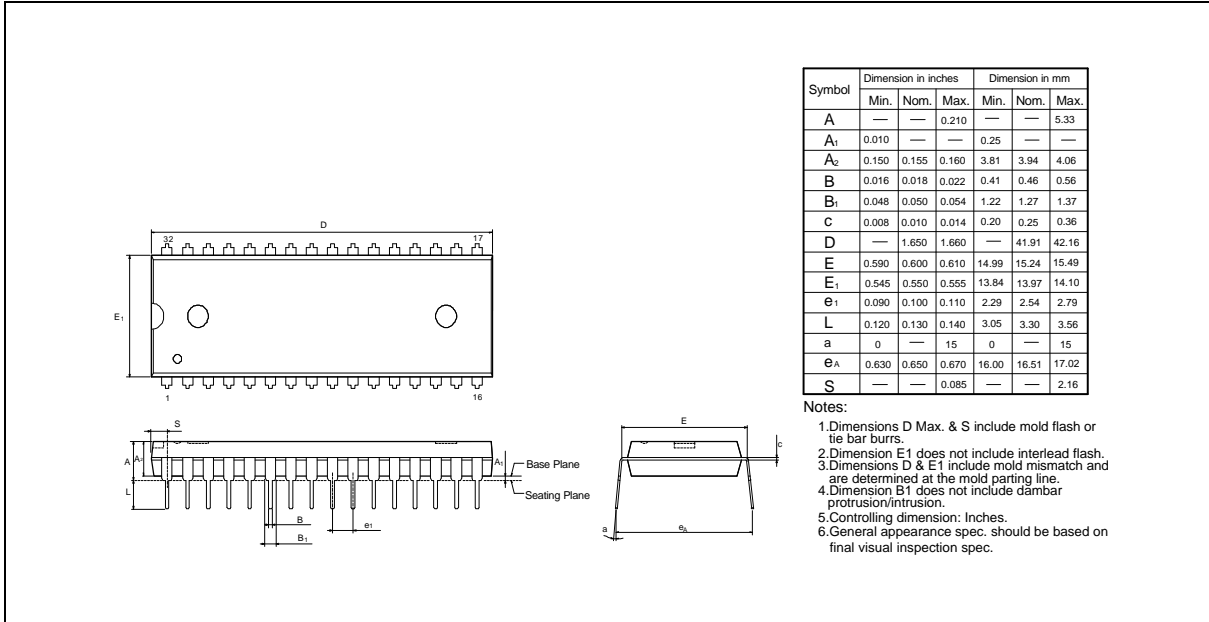
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (mA)	PACKAGE
W29C011A-15	150	50	100	600 mil DIP
W29C011AS-15	150	50	100	450 mil SOP
W29C011AP-15	150	50	100	32-pin PLCC

Notes:

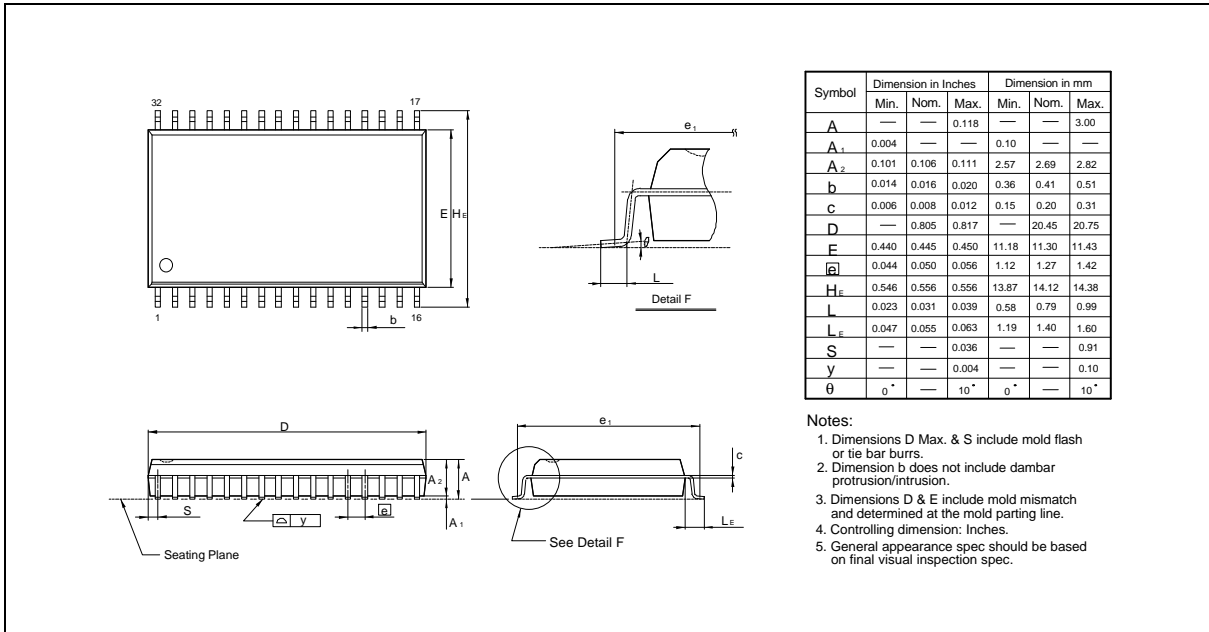
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin P-DIP

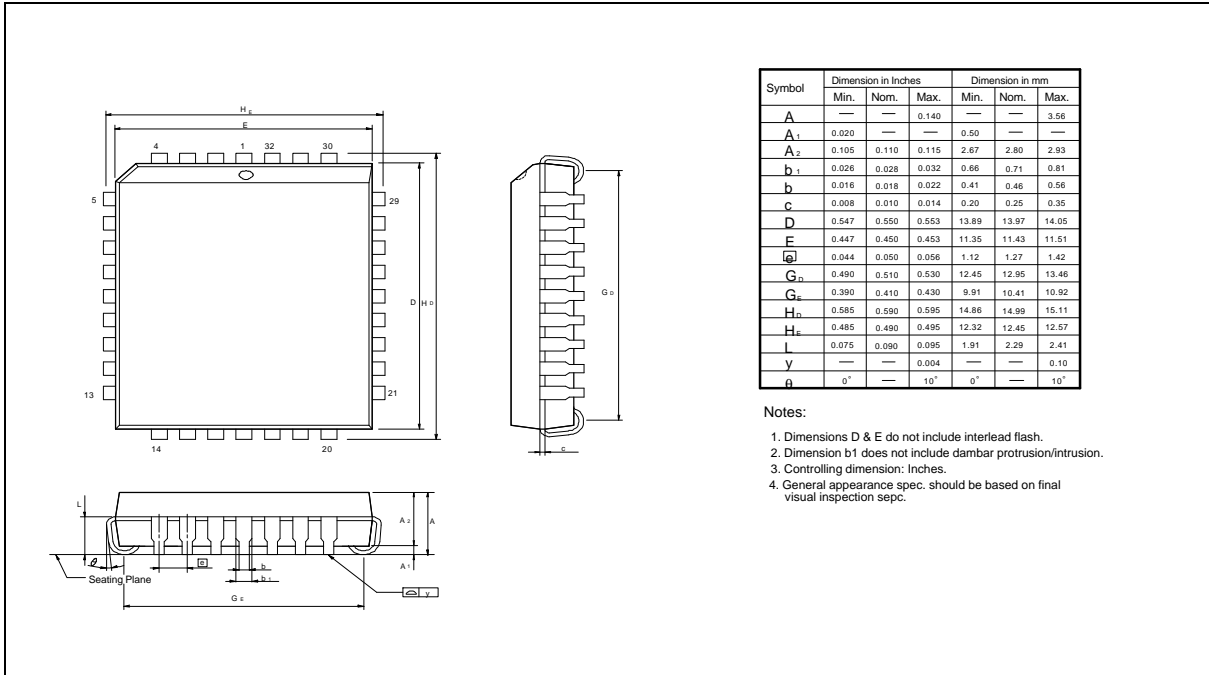


32-pin SO Wide Body



Package Dimensions, continued

32-pin PLCC



VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Dec. 1997		Initial Issued

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Note: All data and specifications are subject to change without notice.

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Revision A1