

INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT
 TC5117405 CSJ / CST - 40
 TC5117405 CSJ / CST - 50
 TC5117405 CSJ / CST - 60
 SILICON GATE CMOS

TENTATIVE DATA

4,194,304 WORD × 4 BIT EDO (HYPER PAGE) DYNAMIC RAM

DESCRIPTION

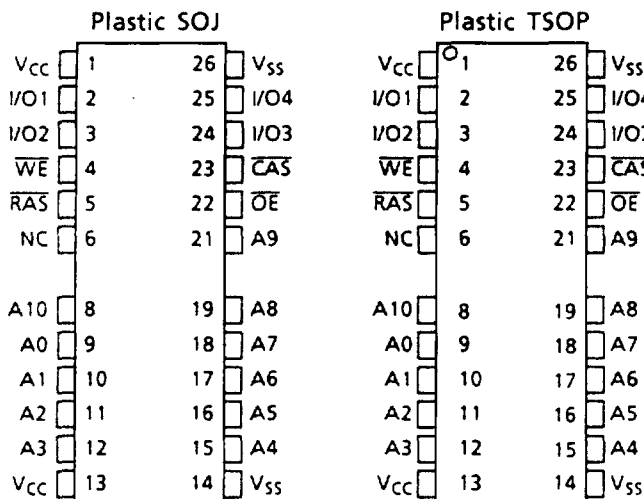
The TC5117405CSJ/CST is EDO (hyper page) dynamic RAM organized 4,194,304 words by 4 bits. The TC5117405CSJ/CST utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5117405CSJ/CST to be packaged in 26/24 pin plastic SOJ (300mil) and 26/24 pin plastic TSOP (300mil). The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low Power
 825mW MAX. Operating (TC5117405CSJ/CST - 40)
 715mW MAX. Operating (TC5117405CSJ/CST - 50)
 605mW MAX. Operating (TC5117405CSJ/CST - 60)
 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, \overline{CAS} before \overline{RAS} refresh, \overline{RAS} -only refresh, Hidden refresh, EDO(Hyper Page Mode) and Test Mode capability
- All inputs and outputs TTL compatible
- 2048 refresh cycles/32ms
- Package TC5117405CSJ : SOJ26-P-300C
 TC5117405CST : TSOP26-P-300D

		TC5117405CSJ/CST		
		- 40	- 50	- 60
t_{RAC}	\overline{RAS} Access Time	40ns	50ns	60ns
t_{AA}	Column Address Access Time	20ns	25ns	30ns
t_{CAC}	\overline{CAS} Access Time	11ns	14ns	17ns
t_{RC}	Cycle Time	69ns	84ns	104ns
t_{HPC}	Hyper Page Mode Cycle Time	16ns	20ns	25ns

PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A10	Address Inputs
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
\overline{WE}	Write Enable
\overline{OE}	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground
NC	No Connection

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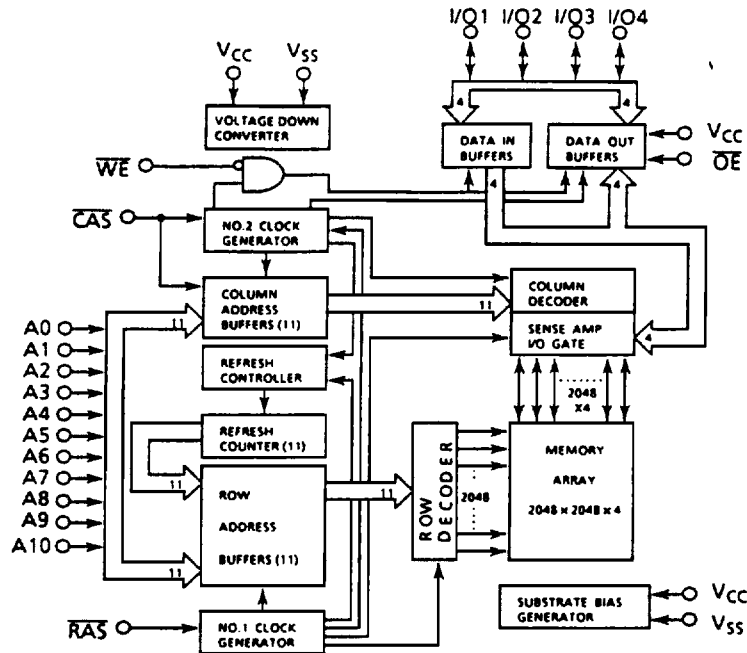
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TC5117405CSJ/CST - 1

1996 - 04 - 01

TOSHIBA CORPORATION

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V	1
Operating Temperature	T_{OPR}	$0 \sim 70$	°C	1
Storage Temperature	T_{STG}	$-55 \sim 150$	°C	1
Soldering Temperature (10s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	900	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	$V_{CC} + 0.5^*$	V	2
V_{IL}	Input Low Voltage	-0.5^{**}	-	0.8	V	2

* $V_{CC} + 2.0\text{V}$ at pulse width $\leq 20\text{ns}$ (pulse width is measured at V_{CC})

** -2.0V at pulse width $\leq 20\text{ns}$ (pulse width is measured at V_{SS})

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I _{CC1}	OPERATING CURRENT Average Power Supply Operating Current (\overline{RAS} , \overline{CAS} , Address Cycling: $t_{RC} = t_{RC} \text{ MIN.}$)	TC5117405CSJ/CST-40	-	150	mA	3, 4 5
		TC5117405CSJ/CST-50	-	130		
		TC5117405CSJ/CST-60	-	110		
I _{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		-	2	mA	
I _{CC3}	\overline{RAS} ONLY REFRESH CURRENT Average Power Supply Current, \overline{RAS} Only Mode (\overline{RAS} Cycling, $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC} \text{ MIN.}$)	TC5117405CSJ/CST-40	-	150	mA	3, 5
		TC5117405CSJ/CST-50	-	130		
		TC5117405CSJ/CST-60	-	110		
I _{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS} = V_{IL}$, \overline{CAS} , Address Cycling: $t_{HPC} = t_{HPC} \text{ MIN.}$)	TC5117405CSJ/CST-40	-	120	mA	3, 4 5
		TC5117405CSJ/CST-50	-	100		
		TC5117405CSJ/CST-60	-	85		
I _{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		-	1	mA	
I _{CC6}	\overline{CAS} BEFORE \overline{RAS} REFRESH CURRENT Average Power Supply Current, \overline{CAS} Before \overline{RAS} Mode (\overline{RAS} , \overline{CAS} Cycling: $t_{RC} = t_{RC} \text{ MIN.}$)	TC5117405CSJ/CST-40	-	150	mA	3, 5
		TC5117405CSJ/CST-50	-	130		
		TC5117405CSJ/CST-60	-	110		
I _{I (L)}	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq V_{CC}$, All Other Pins Not Under Test = 0V)		- 10	10	μA	
I _{O (L)}	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq V_{CC}$)		- 10	10	μA	
V _{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)		2.4	-	V	
V _{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC5117405CSJ/CST						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	69	-	84	-	104	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	92	-	111	-	135	-	ns	
t_{RAC}	Access Time from \overline{RAS}	-	40	-	50	-	60	ns	9, 14, 15
t_{CAC}	Access Time from \overline{CAS}	-	11	-	14	-	17	ns	9, 14
t_{AA}	Access Time from Column Address	-	20	-	25	-	30	ns	9, 15
t_{CPA}	Access Time from \overline{CAS} Precharge	-	22	-	28	-	35	ns	9
t_{CLZ}	\overline{CAS} to output in Low-Z	0	-	0	-	0	-	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	11	0	13	0	15	ns	10, 16
t_T	Transition Time (Rise and Fall)	1	50	1	50	1	50	ns	8
t_{RP}	\overline{RAS} Precharge Time	25	-	30	-	40	-	ns	
t_{RAS}	\overline{RAS} Pulse Width	40	10,000	50	10,000	60	10,000	ns	
t_{RASP}	\overline{RAS} Pulse Width (Hyper Page Mode)	40	200,000	50	200,000	60	200,000	ns	
t_{RSH}	\overline{RAS} Hold Time	6	-	8	-	10	-	ns	
t_{RHCP}	\overline{RAS} Hold Time From \overline{CAS} Precharge (Hyper Page Mode)	22	-	28	-	35	-	ns	
t_{CSH}	\overline{CAS} Hold Time	30	-	35	-	40	-	ns	
t_{CAS}	\overline{CAS} Pulse Width	6	10,000	8	10,000	10	10,000	ns	
t_{RCD}	\overline{RAS} to \overline{CAS} Delay Time	10	29	12	36	14	43	ns	14
t_{RAD}	\overline{RAS} to Column Address Delay Time	8	20	10	25	12	30	ns	15
t_{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	5	-	5	-	5	-	ns	
t_{CP}	\overline{CAS} Precharge Time	6	-	8	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	6	-	8	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	6	-	8	-	10	-	ns	
t_{RAL}	Column Address to \overline{RAS} Lead Time	20	-	25	-	30	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to \overline{RAS}	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	6	-	8	-	10	-	ns	
t_{WP}	Write Command Pulse Width	6	-	8	-	10	-	ns	
t_{RWL}	Write Command to \overline{RAS} Lead Time	6	-	8	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC5117405CSJ/CST						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	6	-	8	-	10	-	ns	
t _{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t _{DH}	Data Hold Time	6	-	8	-	10	-	ns	12
t _{REF}	Refresh Period	-	32	-	32	-	32	ms	
t _{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	26	-	31	-	36	-	ns	13
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	55	-	67	-	79	-	ns	13
t _{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	35	-	42	-	49	-	ns	13
t _{CPWD}	$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	37	-	45	-	54	-	ns	13
t _{CSR}	$\overline{\text{CAS}}$ Set-Up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	5	-	5	-	5	-	ns	
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	6	-	8	-	10	-	ns	
t _{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	5	-	5	-	5	-	ns	
t _{CPT}	$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Counter Test Cycle)	20	-	20	-	20	-	ns	
t _{ROH}	$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	6	-	8	-	10	-	ns	
t _{OE A}	$\overline{\text{OE}}$ Access Time	-	11	-	13	-	15	ns	9
t _{OE D}	$\overline{\text{OE}}$ to Data Delay	11	-	13	-	15	-	ns	
t _{OLZ}	$\overline{\text{OE}}$ to output in Low-Z	0	-	0	-	0	-	ns	
t _{OE Z}	Output buffer turn off Delay Time from $\overline{\text{OE}}$	0	11	0	13	0	15	ns	10
t _{OE H}	$\overline{\text{OE}}$ Command Hold Time	6	-	8	-	10	-	ns	
t _{ODS}	Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t _{WTS}	Write Command Set-Up Time (Test Mode In)	5	-	5	-	5	-	ns	
t _{WTH}	Write Command Hold Time (Test Mode In)	6	-	8	-	10	-	ns	
t _{WRP}	$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	5	-	5	-	5	-	ns	
t _{WRH}	$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	6	-	8	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

SYMBOL	PARAMETER	TC5117405CSJ/CST						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RNCD}	\overline{RAS} to next \overline{CAS} Delay Time (Hyper Page Mode)	40	-	50	-	60	-	ns	
t _{HPC}	Hyper Page Mode Cycle Time	16	-	20	-	25	-	ns	
t _{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	47	-	57	-	68	-	ns	
t _{COH}	Output Data Hold Time	5	-	5	-	5	-	ns	
t _{REZ}	Output Buffer Turn-off Delay from \overline{RAS}	0	11	0	13	0	15	ns	10, 16
t _{WEZ}	Output Buffer Turn-off Delay from \overline{WE}	0	11	0	13	0	15	ns	10
t _{WED}	\overline{WE} to Data Delay	11	-	13	-	15	-	ns	
t _{OE}	\overline{OE} Pulse Width	11	-	13	-	15	-	ns	
t _{OEP}	\overline{OE} Precharge Time	6	-	8	-	10	-	ns	
t _{CPO}	\overline{CAS} to \overline{OE} Precharge Time	5	-	5	-	5	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC5117405CSJ/CST						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read or Write Cycle Time	74	-	89	-	109	-	ns	
t _{HPC}	Hyper Page Mode Cycle Time	21	-	25	-	30	-	ns	
t _{RAC}	Access Time from \overline{RAS}	-	45	-	55	-	65	ns	9,14,15
t _{CAC}	Access Time from \overline{CAS}	-	16	-	19	-	22	ns	9,14
t _{AA}	Access Time from Column Address	-	25	-	30	-	35	ns	9,15
t _{CPA}	Access Time from \overline{CAS} Precharge	-	27	-	33	-	40	ns	9
t _{RAS}	\overline{RAS} Pulse Width	45	10,000	55	10,000	65	10,000	ns	
t _{RASP}	\overline{RAS} Pulse Width (Hyper Page Mode)	45	200,000	55	200,000	65	200,000	ns	
t _{RSH}	\overline{RAS} Hold Time	11	-	13	-	15	-	ns	
t _{CSH}	\overline{CAS} Hold Time	35	-	40	-	45	-	ns	
t _{RHCP}	\overline{CAS} Precharge to \overline{RAS} Hold Time	27	-	33	-	40	-	ns	
t _{CAS}	\overline{CAS} Pulse Width	11	10,000	13	10,000	15	10,000	ns	
t _{RAL}	Column Address to \overline{RAS} Lead Time	25	-	30	-	35	-	ns	

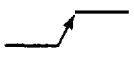


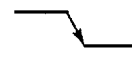
CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $f = 1MHz$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{i1}	Input Capacitance (A0~A10)	-	5	pF
C _{i2}	Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{WE} , \overline{OE})	-	7	pF
C _o	Input/Output Capacitance (I/O1~I/O4)	-	7	pF

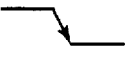

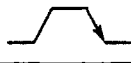
NOTES:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} depend on cycle rate.
4. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed once or less while $\overline{RAS} = V_{IL}$. In case of I_{CC4} , it can be changed once or less during a hyper page mode cycle (t_{HPC}).
6. An initial pause of $200\mu s$ is required after power-up following by 8 \overline{RAS} only refresh cycles before proper operating is achieved. In case of using internal refresh counter, a minimum of 8 \overline{CAS} before \overline{RAS} refresh cycles instead of 8 \overline{RAS} only refresh cycles are required.
7. AC measurement assume $t_T = 2ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.), t_{OEZ} (max.), t_{REZ} (max.) and t_{WEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in Read-Modify-Write cycles.
13. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{AWD} \geq t_{AWD}(\text{min.})$ and $t_{CPWD} \geq t_{CPWD}(\text{min.})$ (Hyper Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met.
 $t_{RCD}(\text{max.})$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
15. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met.
 $t_{RAD}(\text{max.})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
16. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going (t_{OFF}). If \overline{CAS} goes to high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going (t_{REZ}).

Data Out Hi-Z control Logic

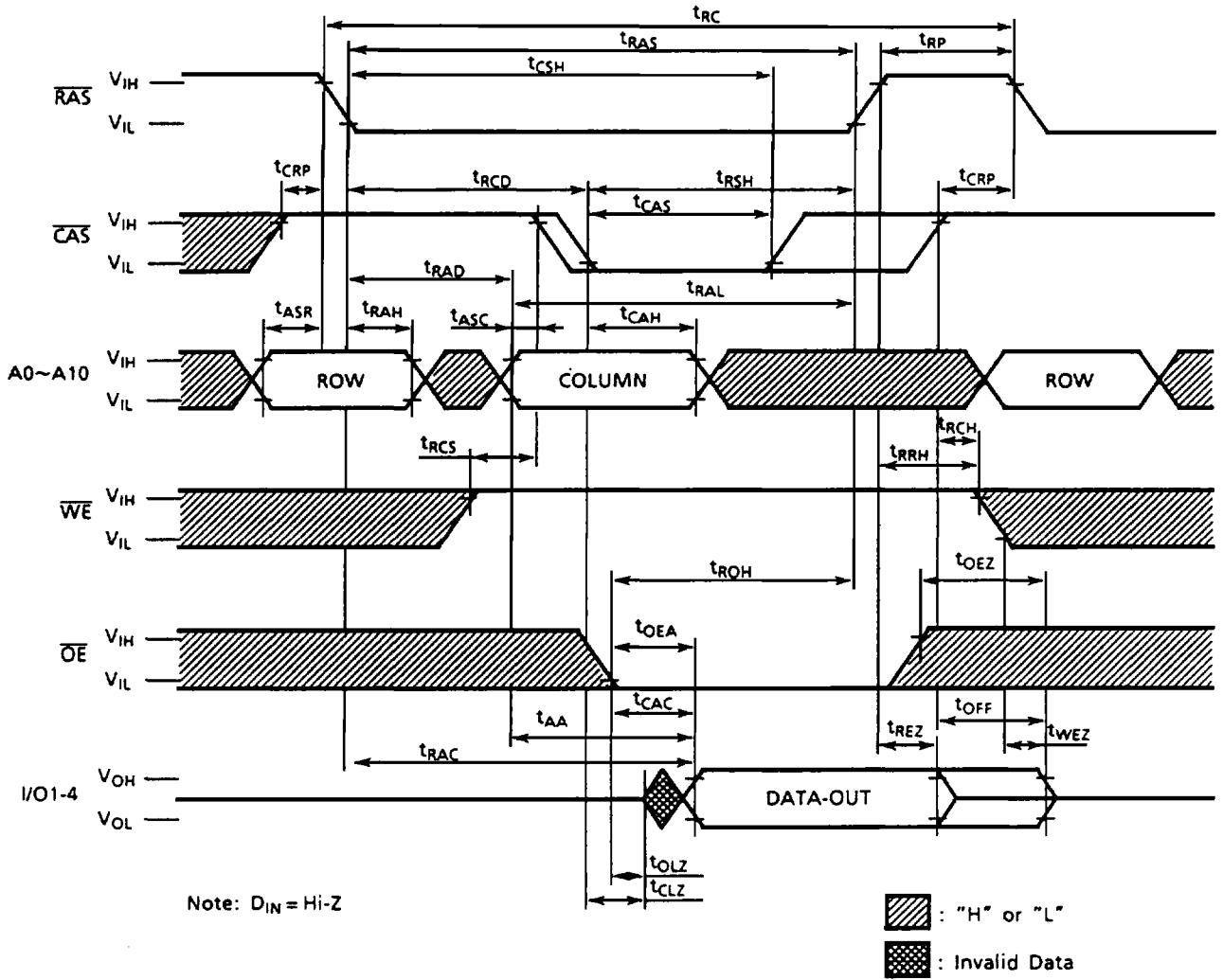
\overline{RAS}	\overline{CAS}	\overline{OE}	\overline{WE}	Timing Specification
"H"		"L"	"H"	t_{OFF}
	"H"	"L"	"H"	t_{REZ}
"L"	"L"		"H"	t_{OEZ}
"L"	"H"	"L"		t_{WEZ}

Data Out Lo-Z control Logic

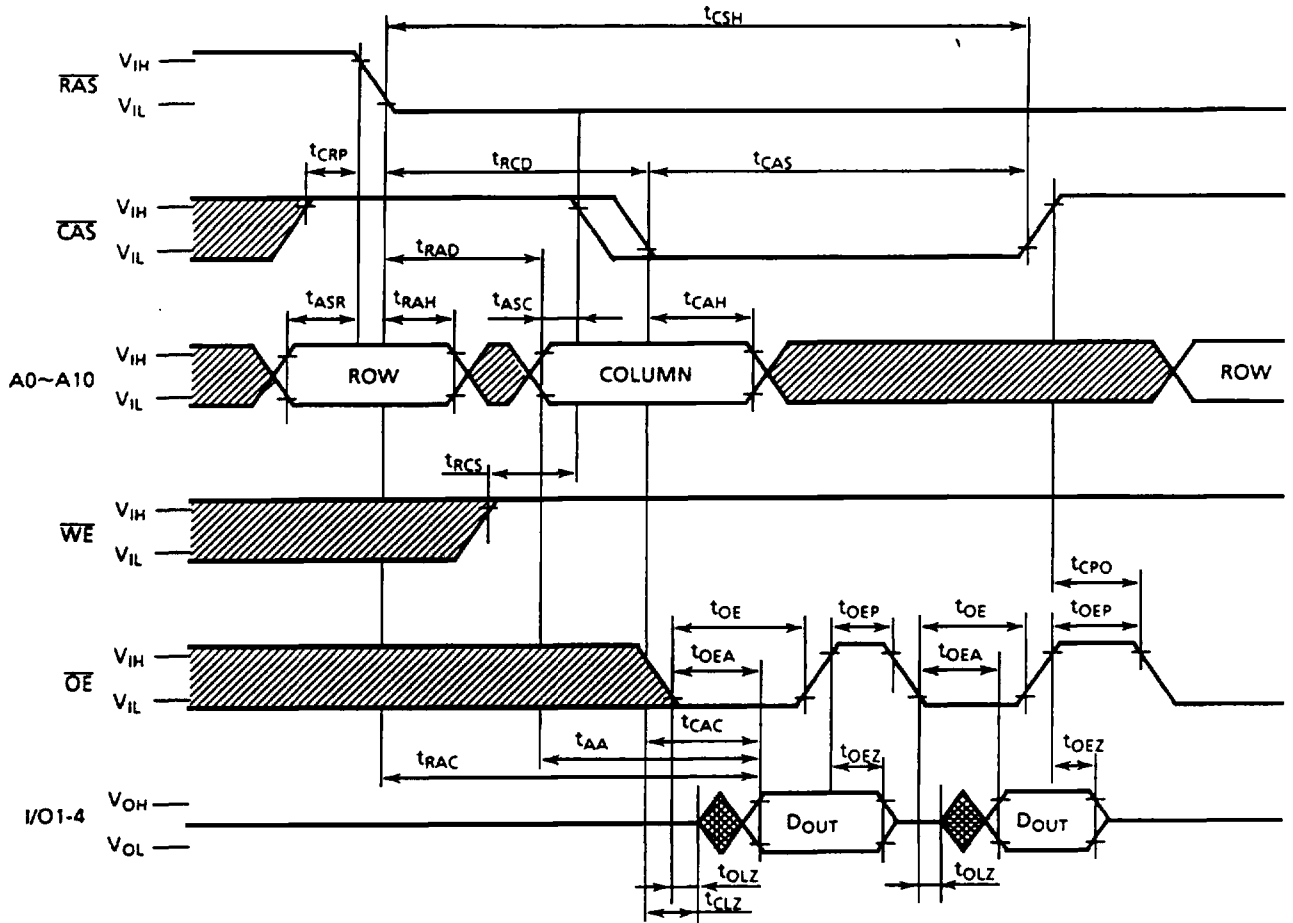
\overline{RAS}	\overline{CAS}	\overline{OE}	\overline{WE}	Timing Specification
"L"		"L"	"H"	t_{CLZ}
"L"	"L"		"H"	t_{OLZ}
"L"	"L"		"H"	t_{OLZ}

TIMING DIAGRAMS

READ CYCLE



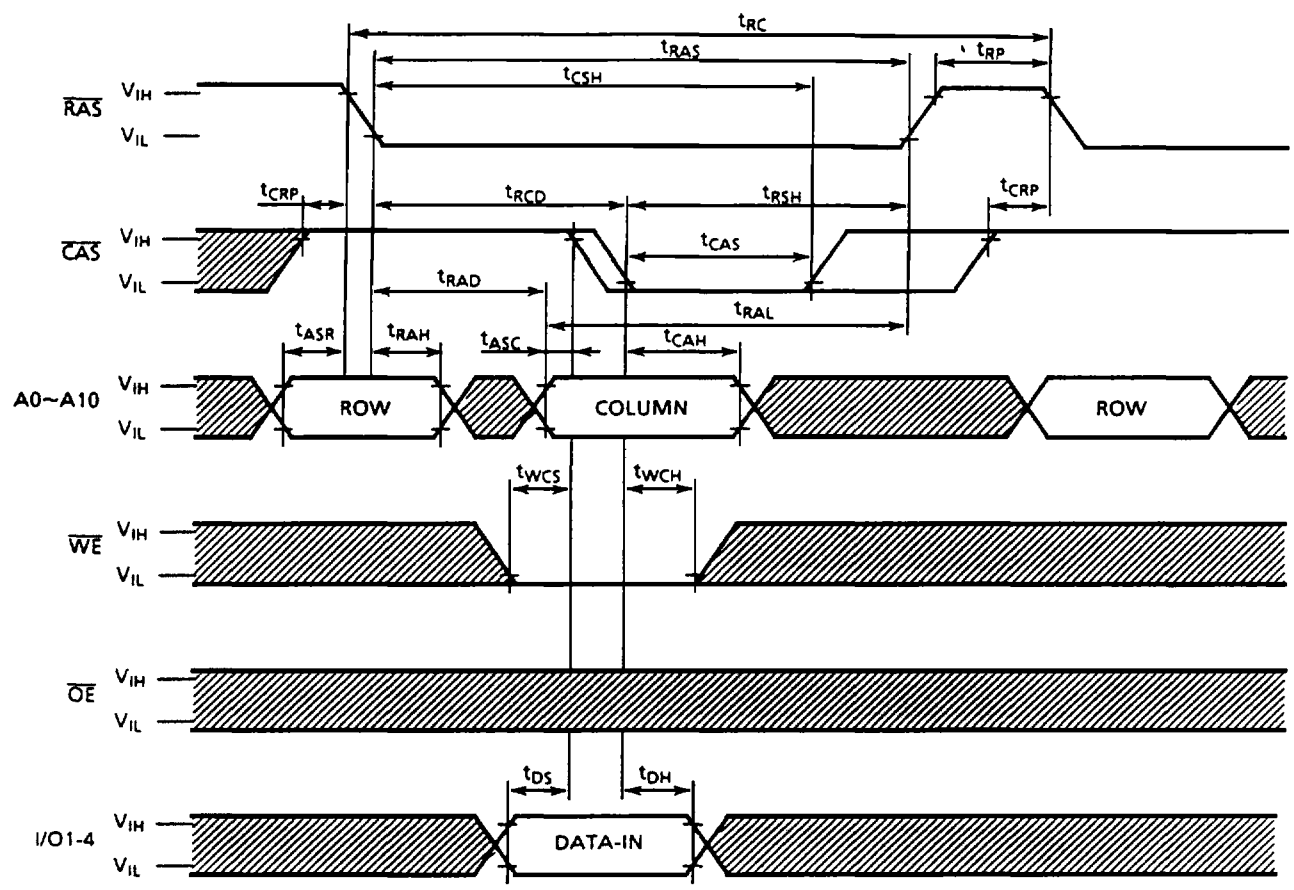
READ CYCLE (\overline{OE} CONTROL)



Note : $D_{IN} = Hi-Z$

▨ : "H" or "L"
▩ : Invalid Data

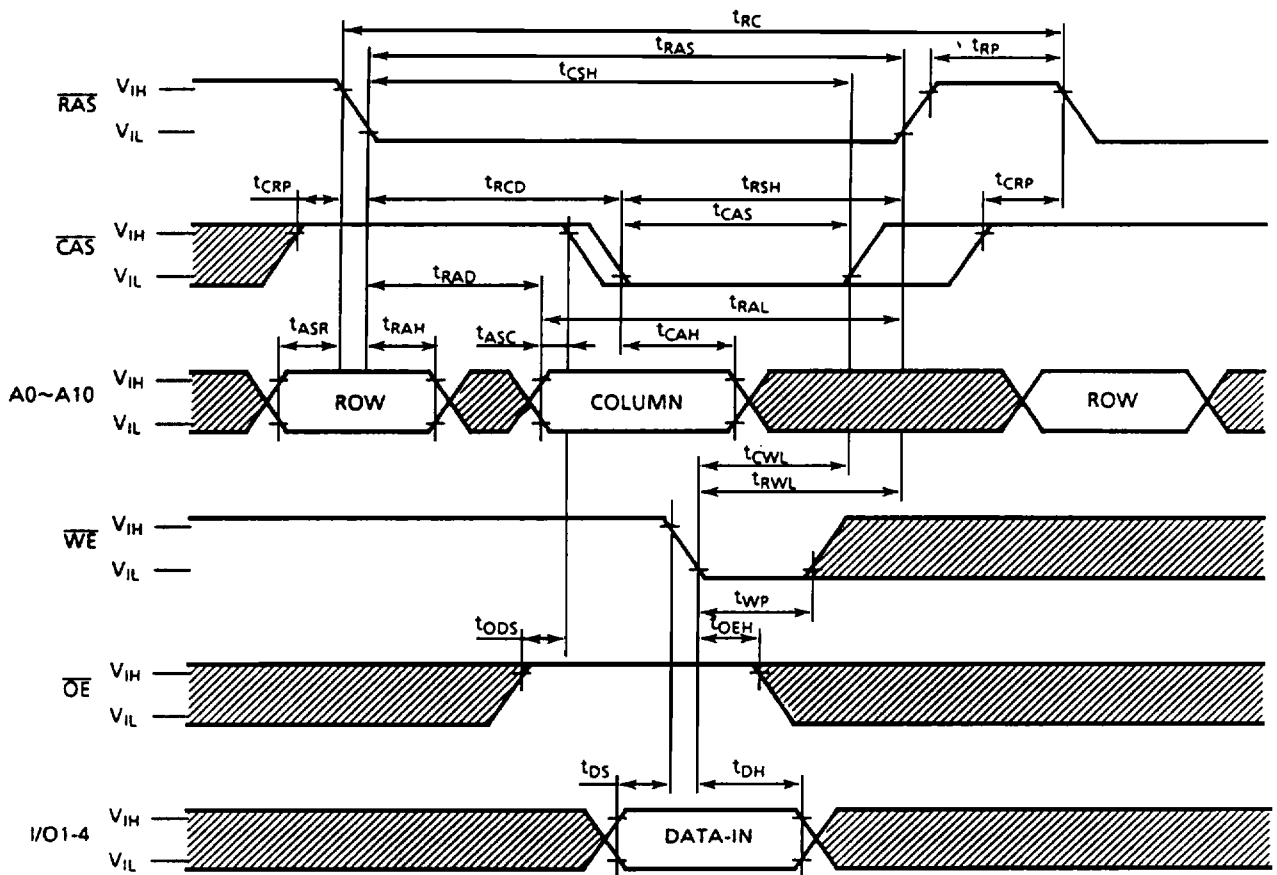
WRITE CYCLE (EARLY WRITE)




Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

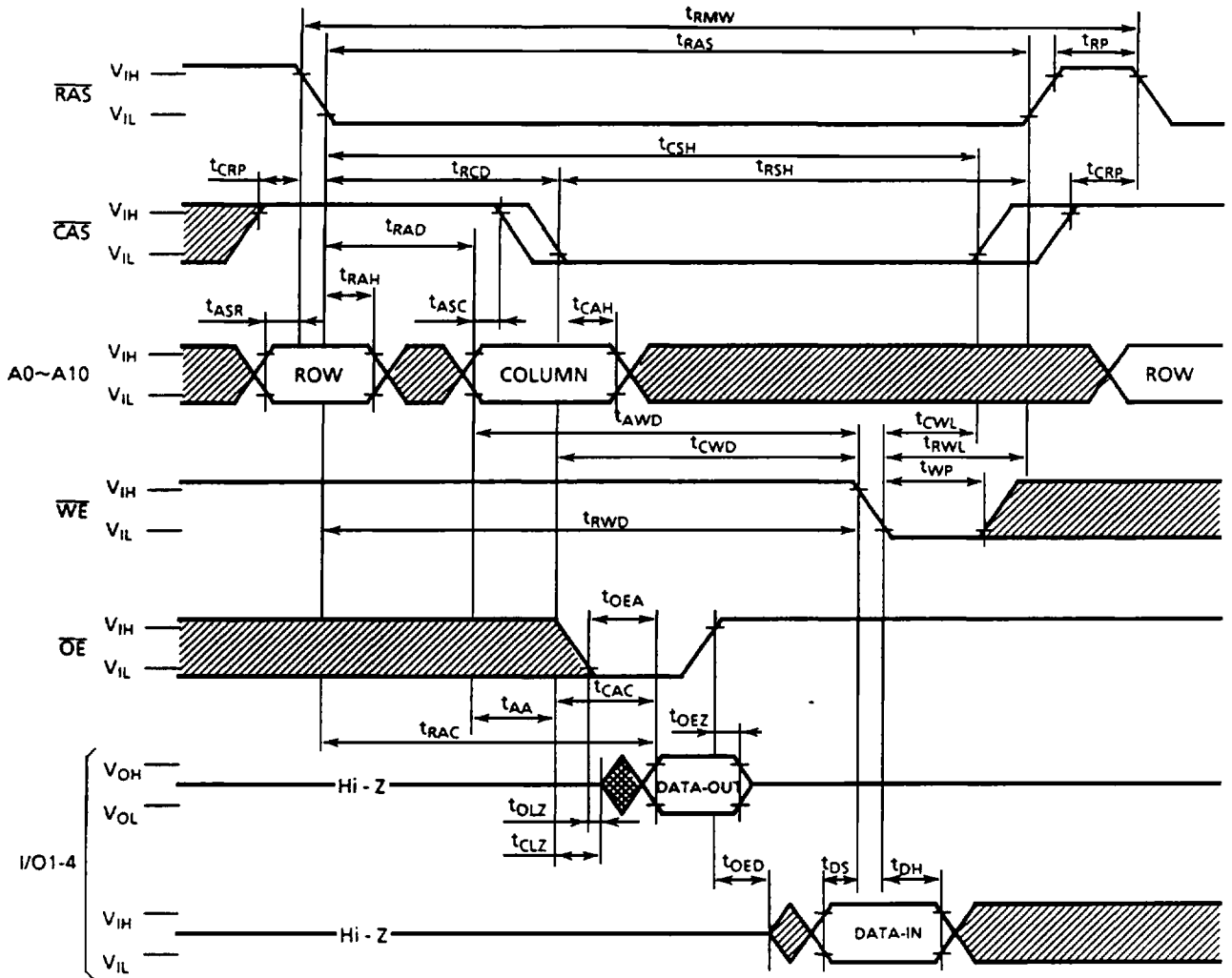
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



Note: $D_{OUT} = Hi-Z$

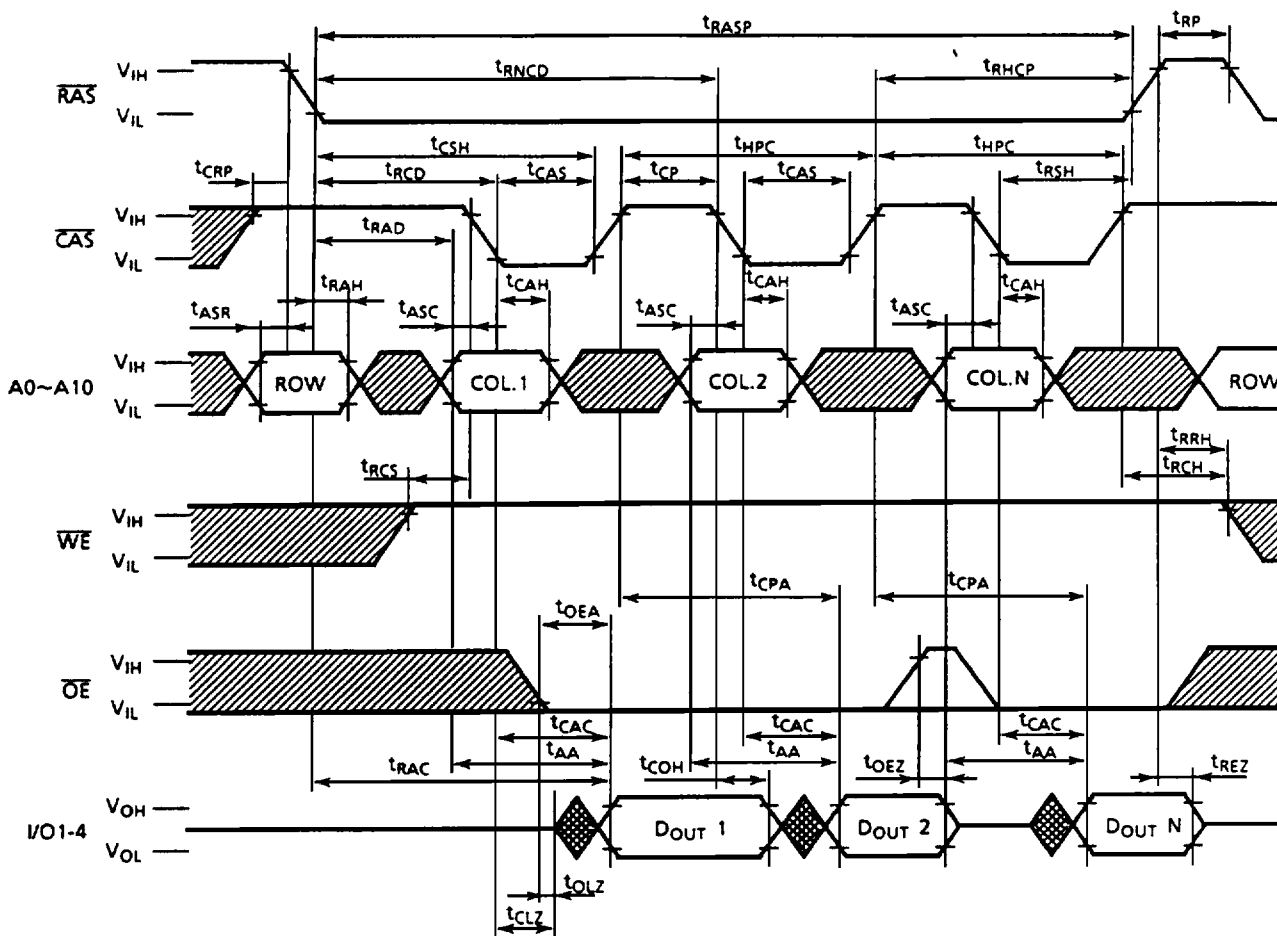
 : "H" or "L"

READ-MODIFY-WRITE CYCLE



▨ : "H" or "L"
▩ : Invalid Data

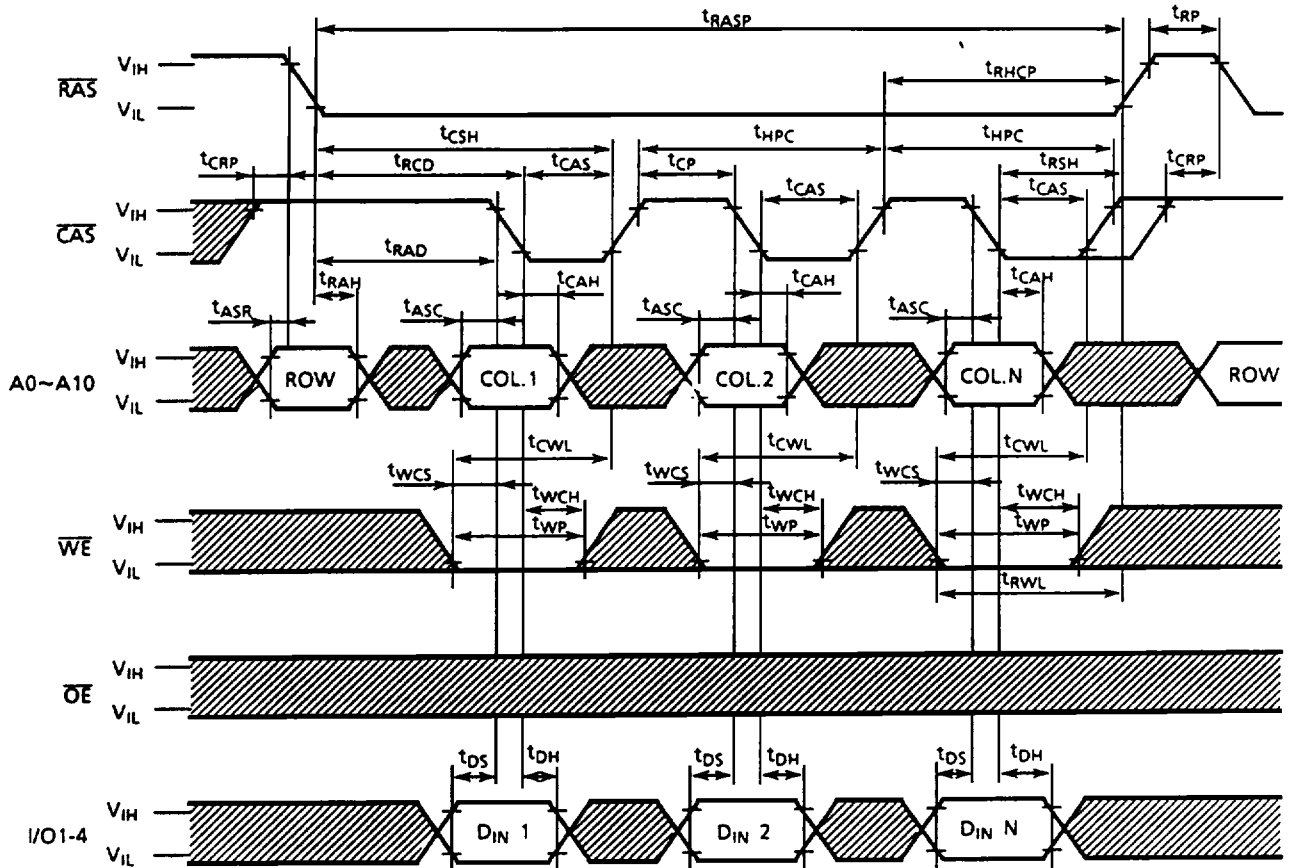
HYPER PAGE MODE READ CYCLE




Note: $D_{IN} = Hi-Z$

▨ : "H" or "L"
▩ : Invalid Data

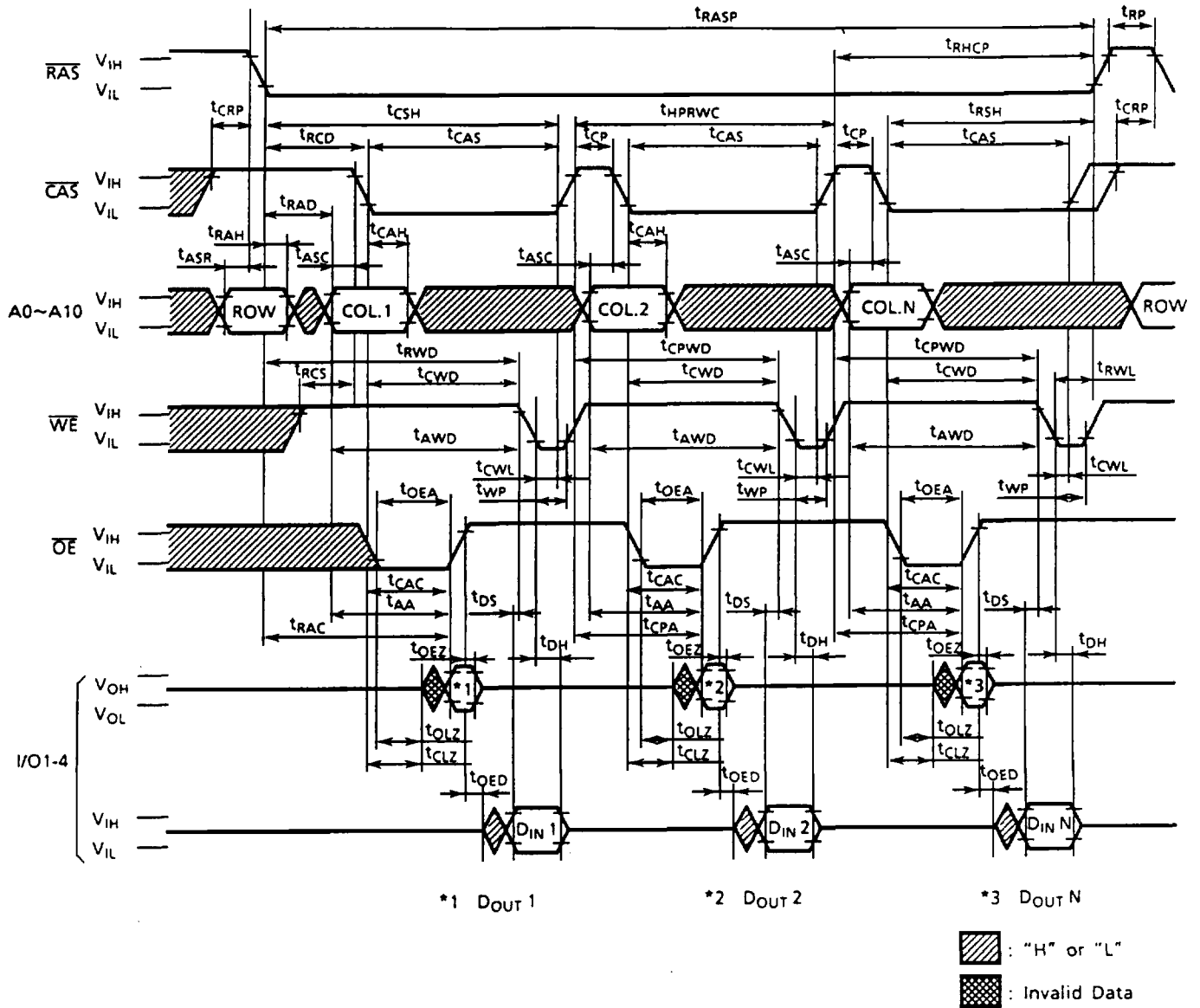
HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



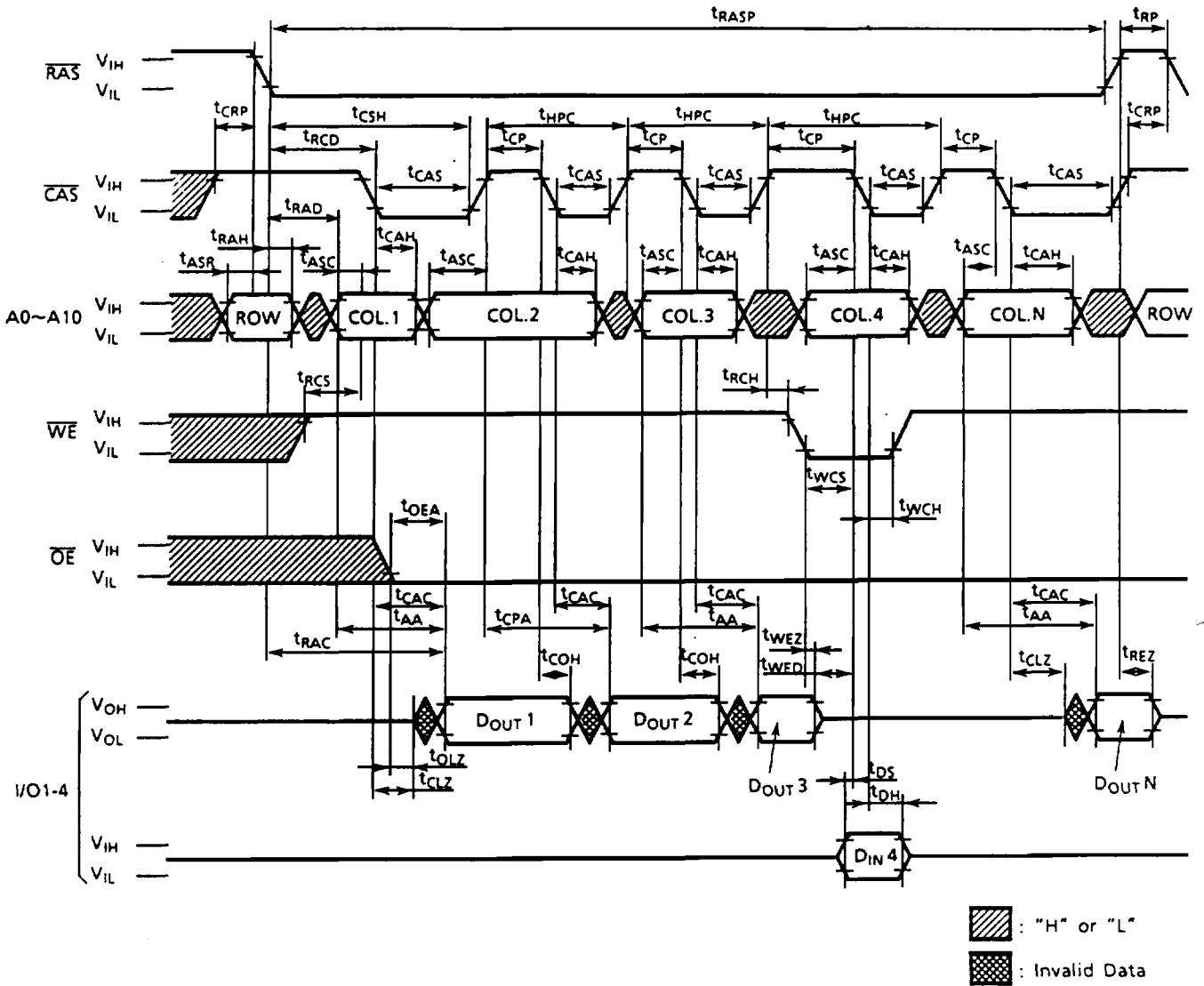
Note: D_{OUT} = Hi-Z

 : "H" or "L"

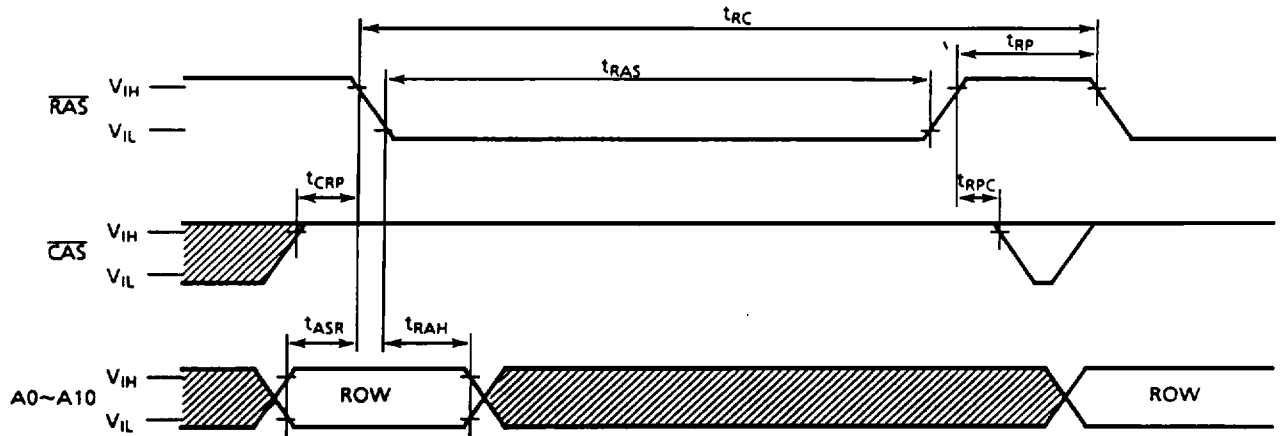
HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE READ WRITE MIXED CYCLE



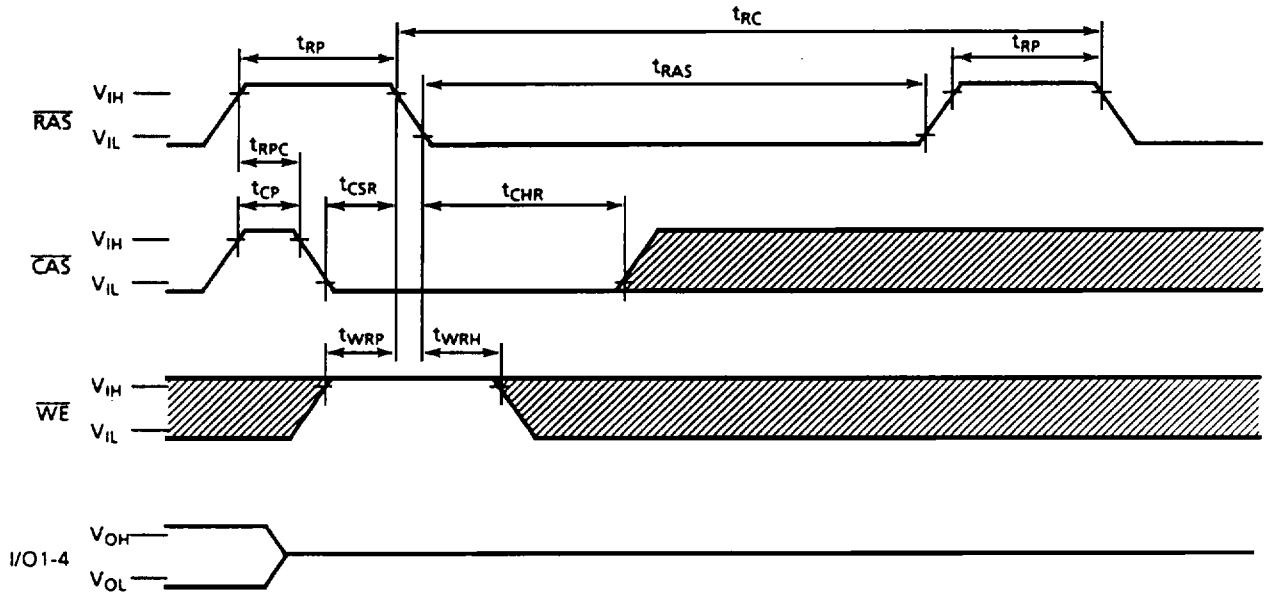
RAS ONLY REFRESH CYCLE



Note: D_{IN} , $\overline{\text{WE}}$, $\overline{\text{OE}}$ = "H" or "L"

▨ : "H" or "L"

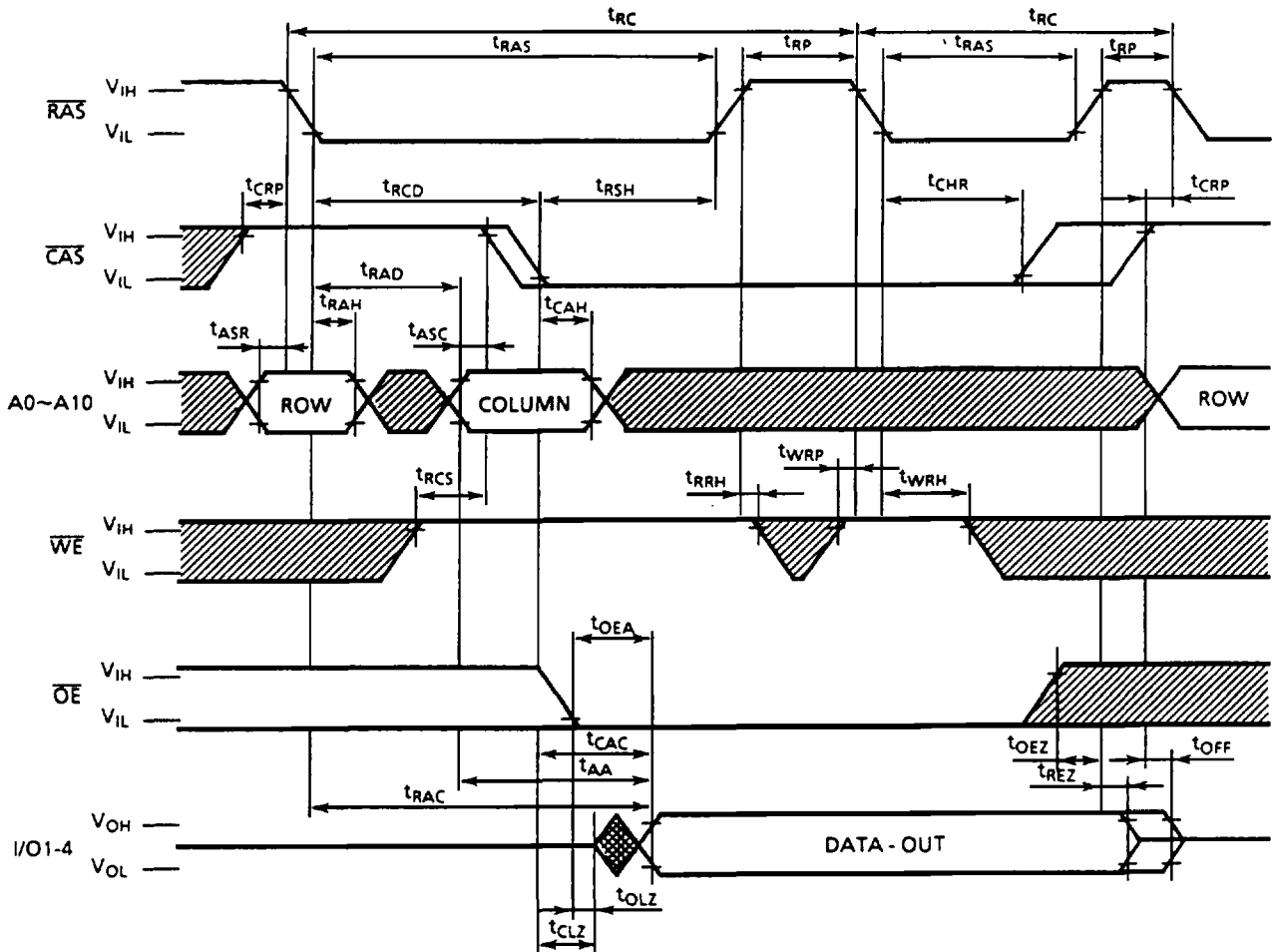
CAS BEFORE RAS REFRESH CYCLE



Note: D_{IN} , $\overline{\text{OE}}$, $\text{A0} \sim \text{A11}$ = "H" or "L"

▨ : "H" or "L"

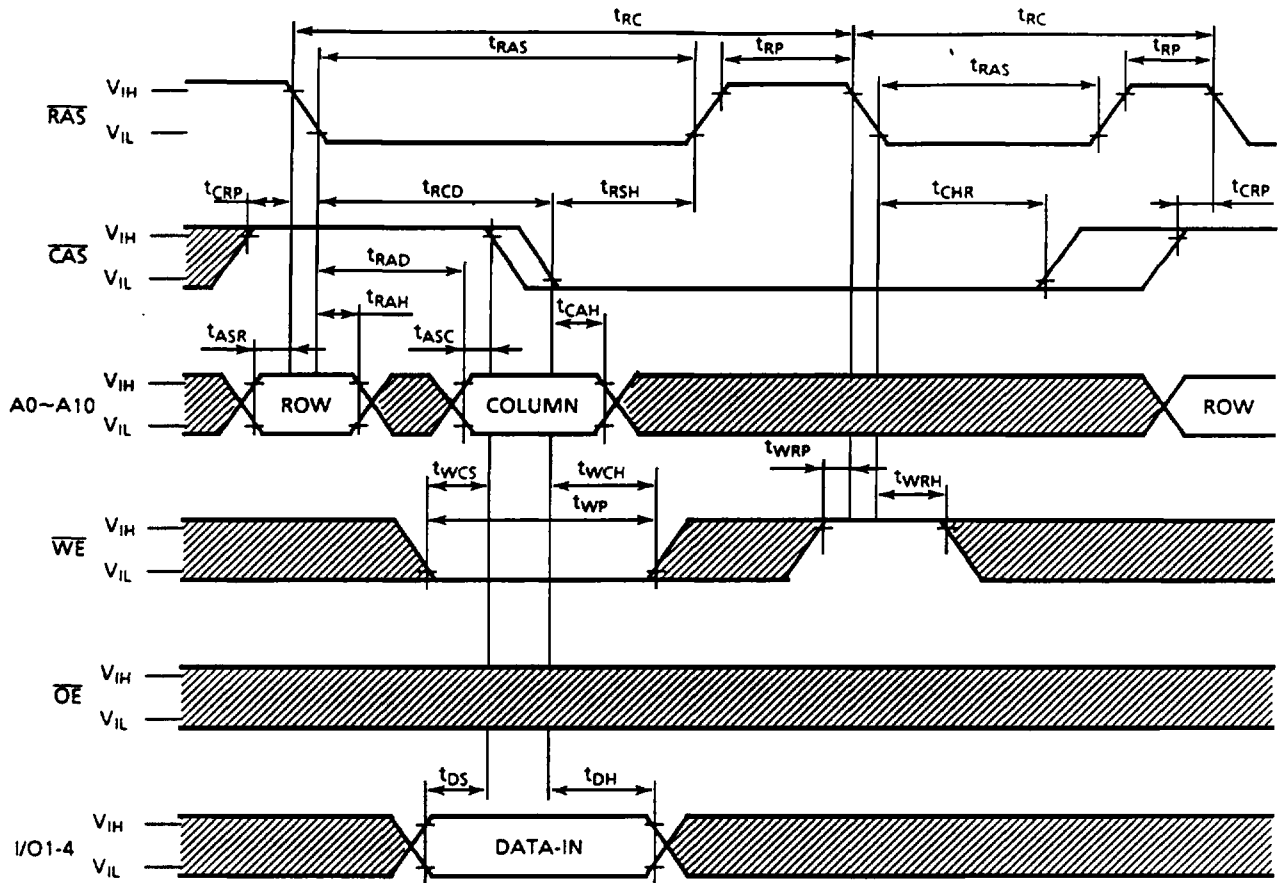
HIDDEN REFRESH CYCLE (READ)



Note : $D_{IN} = Hi-Z$

▨ : "H" or "L"
▩ : Invalid Data

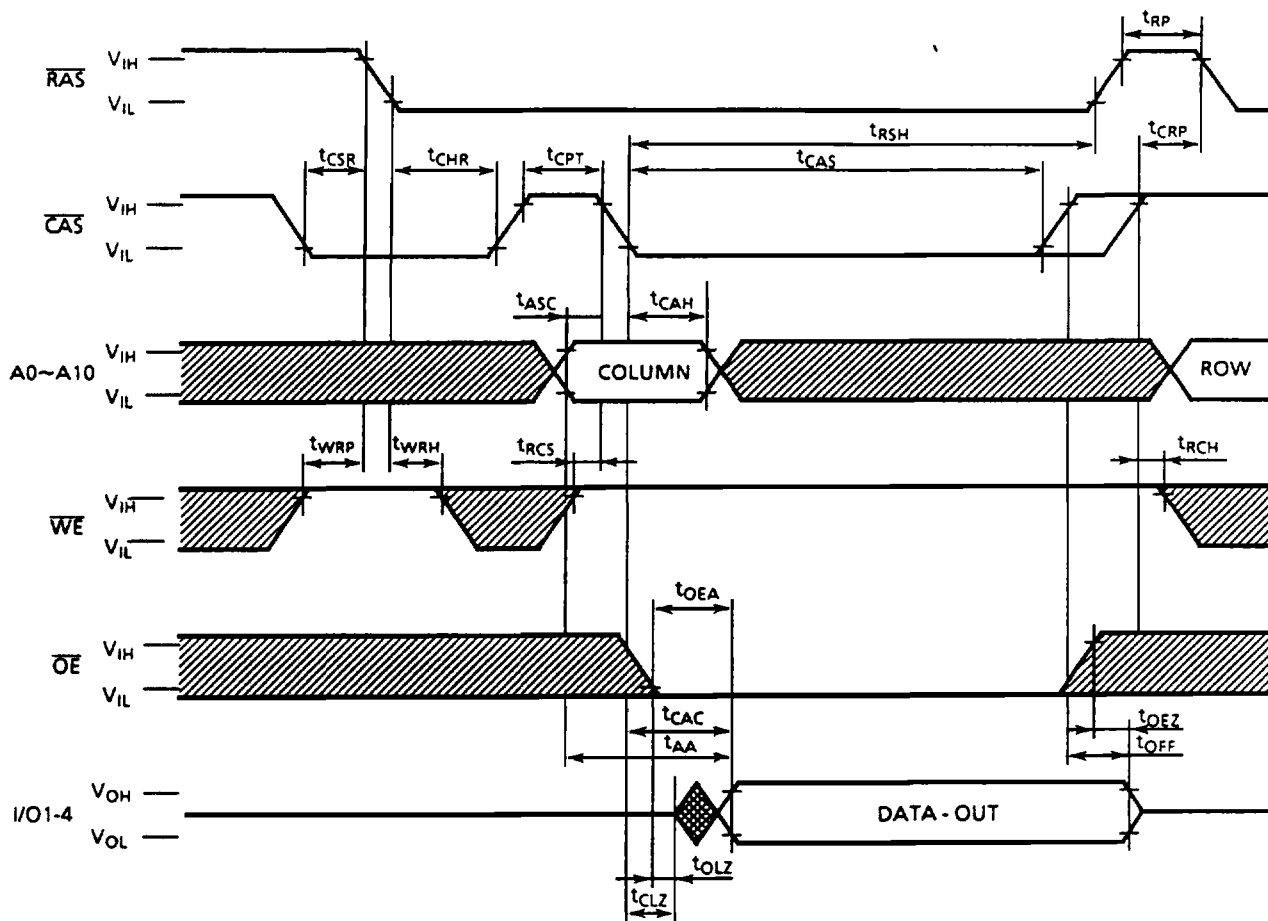
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

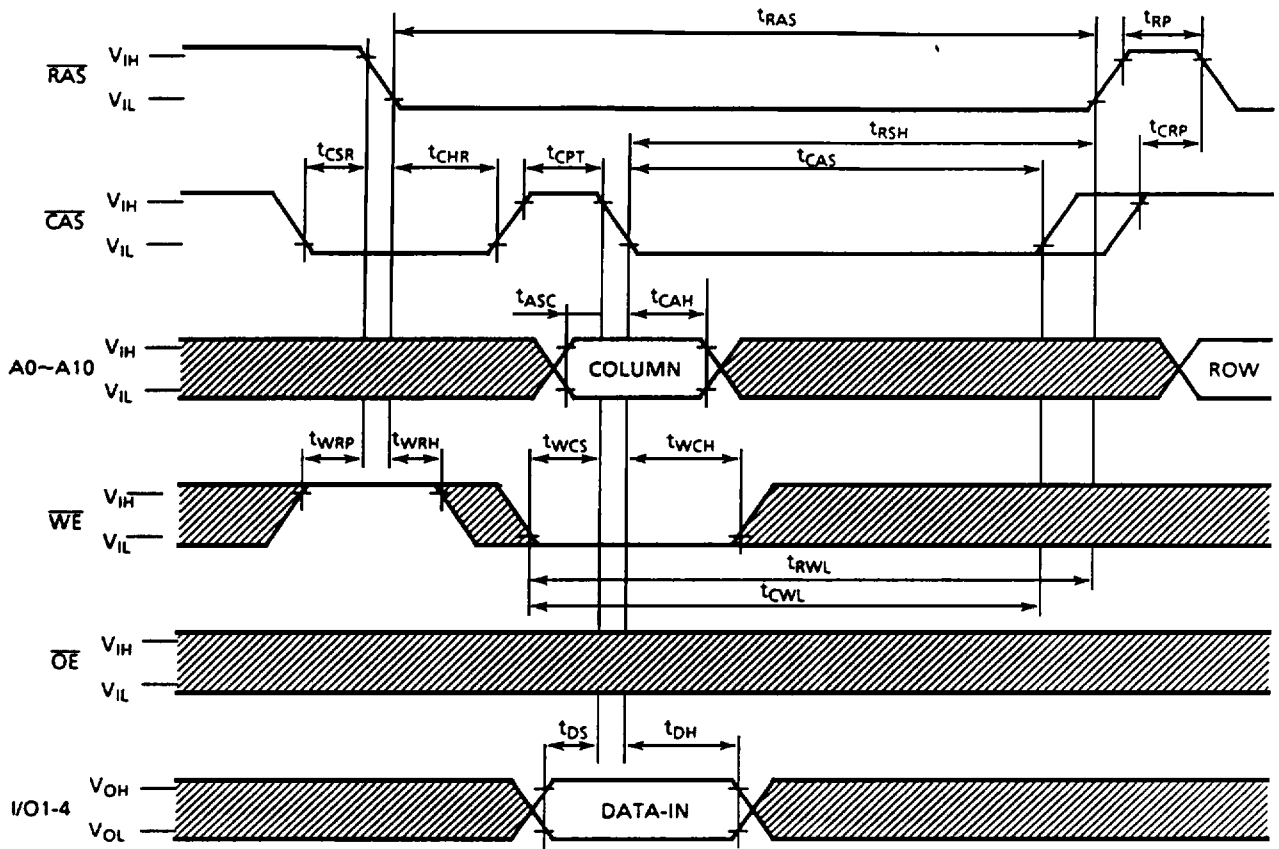
CBR COUNTER TEST CYCLE (READ)



Note: $D_{IN} = \text{Hi-Z}$

▨ : "H" or "L"
▩ : Invalid Data

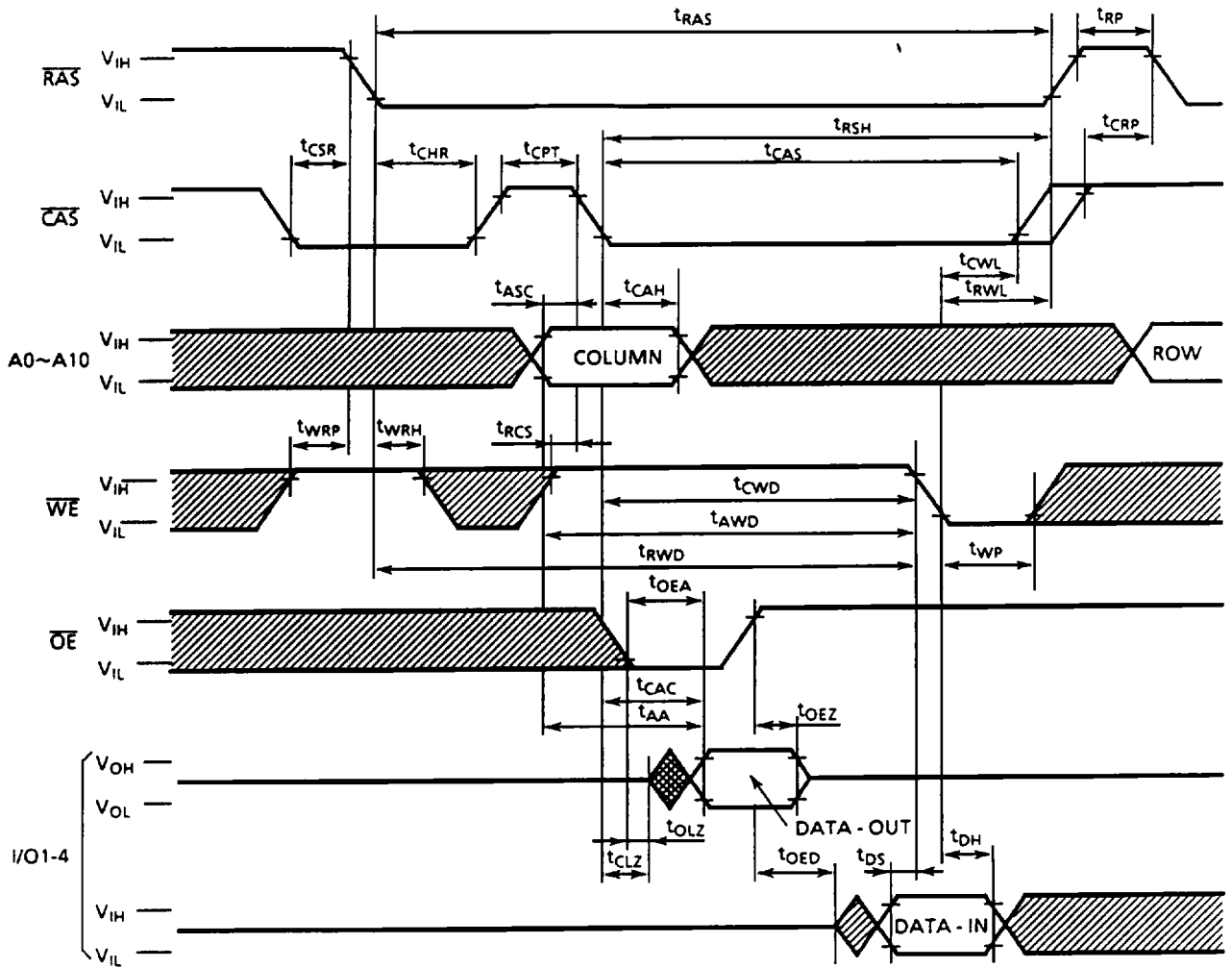
CBR COUNTER TEST CYCLE (WRITE)



Note: DOUT = Hi-Z

▨ : "H" or "L"

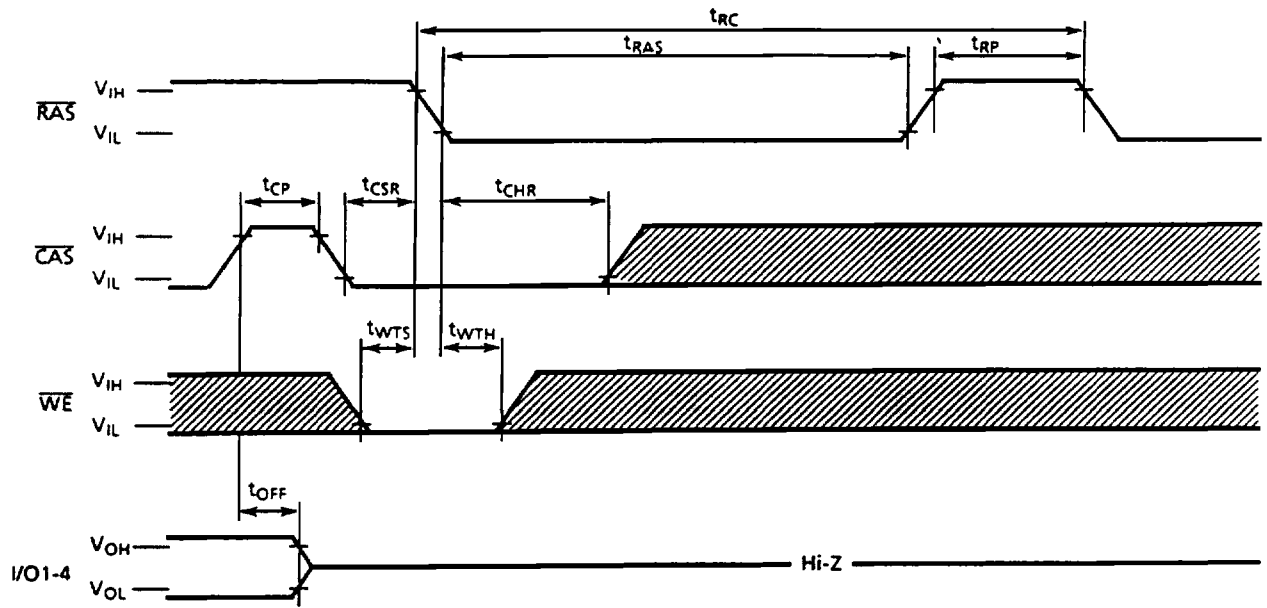
CBR COUNTER TEST CYCLE (READ-MODIFY-WRITE)



Note: $D_{IN} = Hi-Z$

▨ : "H" or "L"
▩ : Invalid Data

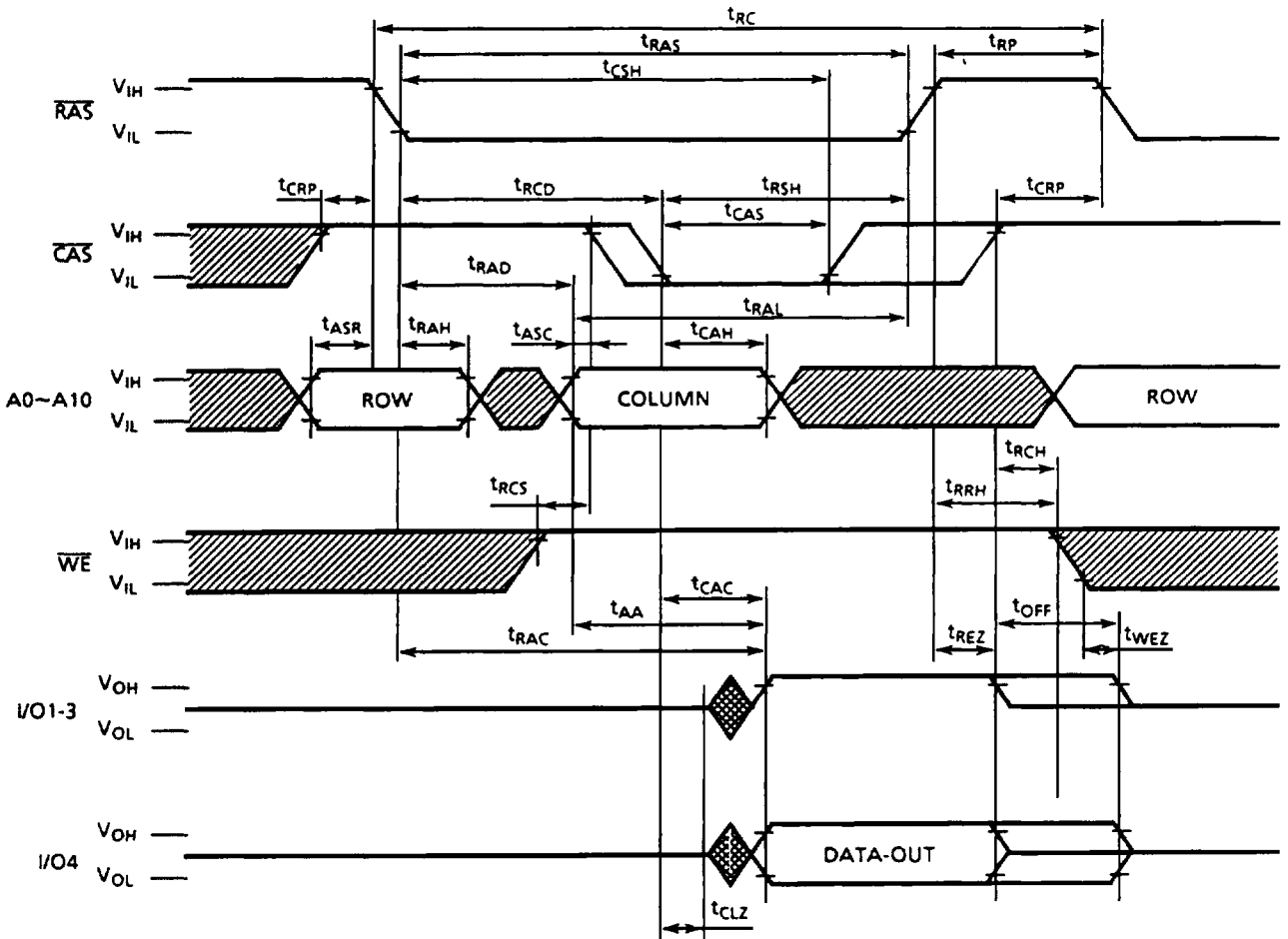
WE, CAS BEFORE RAS REFRESH CYCLE



Note : D_{IN} , \overline{OE} , A0~A11 = "H" or "L"

▨ : "H" or "L"

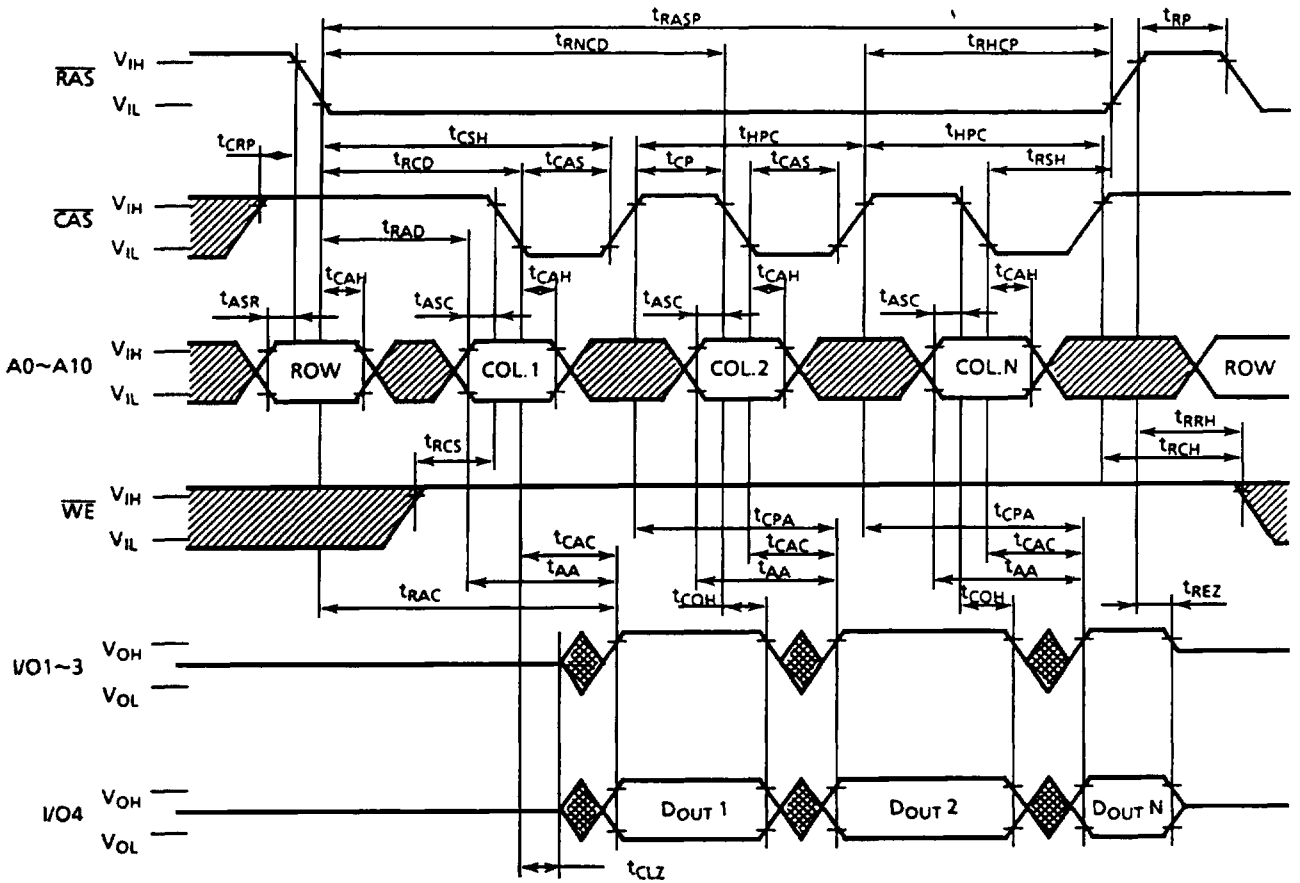
READ CYCLE IN THE TEST MODE



Note : $\overline{OE} = "L"$, $D_{IN} = \text{Hi-Z}$

▨ : "H" or "L"
 ▩ : Invalid Data

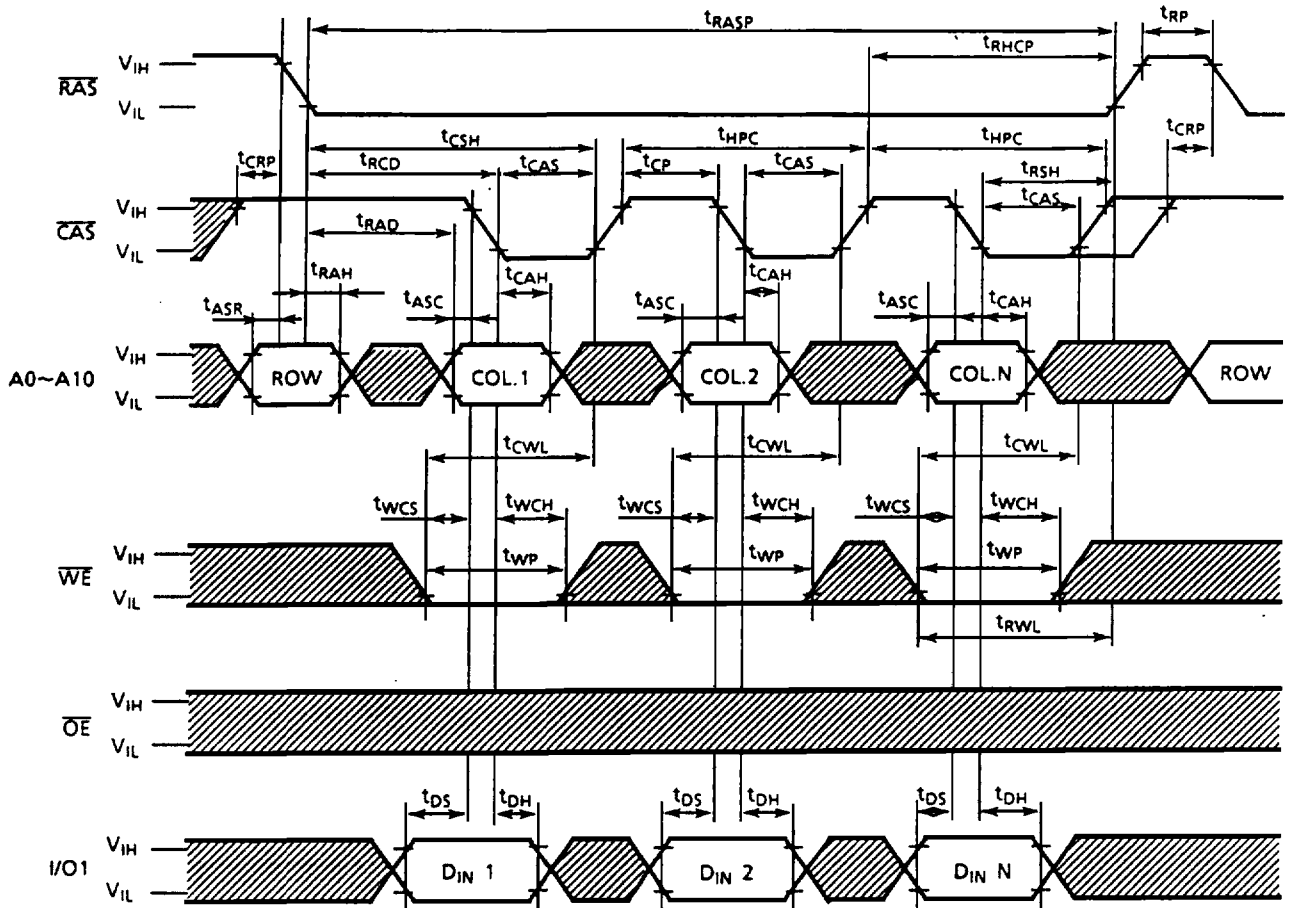
HYPER PAGE MODE READ CYCLE IN THE TEST MODE



Note: $\overline{OE} = "L"$, $D_{IN} = \text{Hi-Z}$

▨ : "H" or "L"
 ▩ : Invalid Data

HYPER PAGE MODE WRITE CYCLE IN THE TEST MODE



Note: I/O2-4 = "H" or "L", D_{OUT} = Hi-Z

▨ : "H" or "L"

TEST MODE

The TC5117405CSJ/CST is the RAM organized 4,194,304 words by 4 bits, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel by using only I/O1. A1c, A0c are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s), the I/O4 pin indicates a "1". If they were not equal, the I/O4 pin would indicate a "0". I/O1, I/O2 and I/O3 always indicate a "1" during test mode read cycle. Fig.1 shows the block diagram of TC5117405CSJ/CST. In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×16 DRAM.

" \overline{WE} , \overline{CAS} Before \overline{RAS} Refresh Cycle" puts the device into "Test Mode". And " \overline{CAS} Before \overline{RAS} Refresh Cycle" or " \overline{RAS} Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " \overline{WE} , \overline{CAS} Before \overline{RAS} Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/4 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

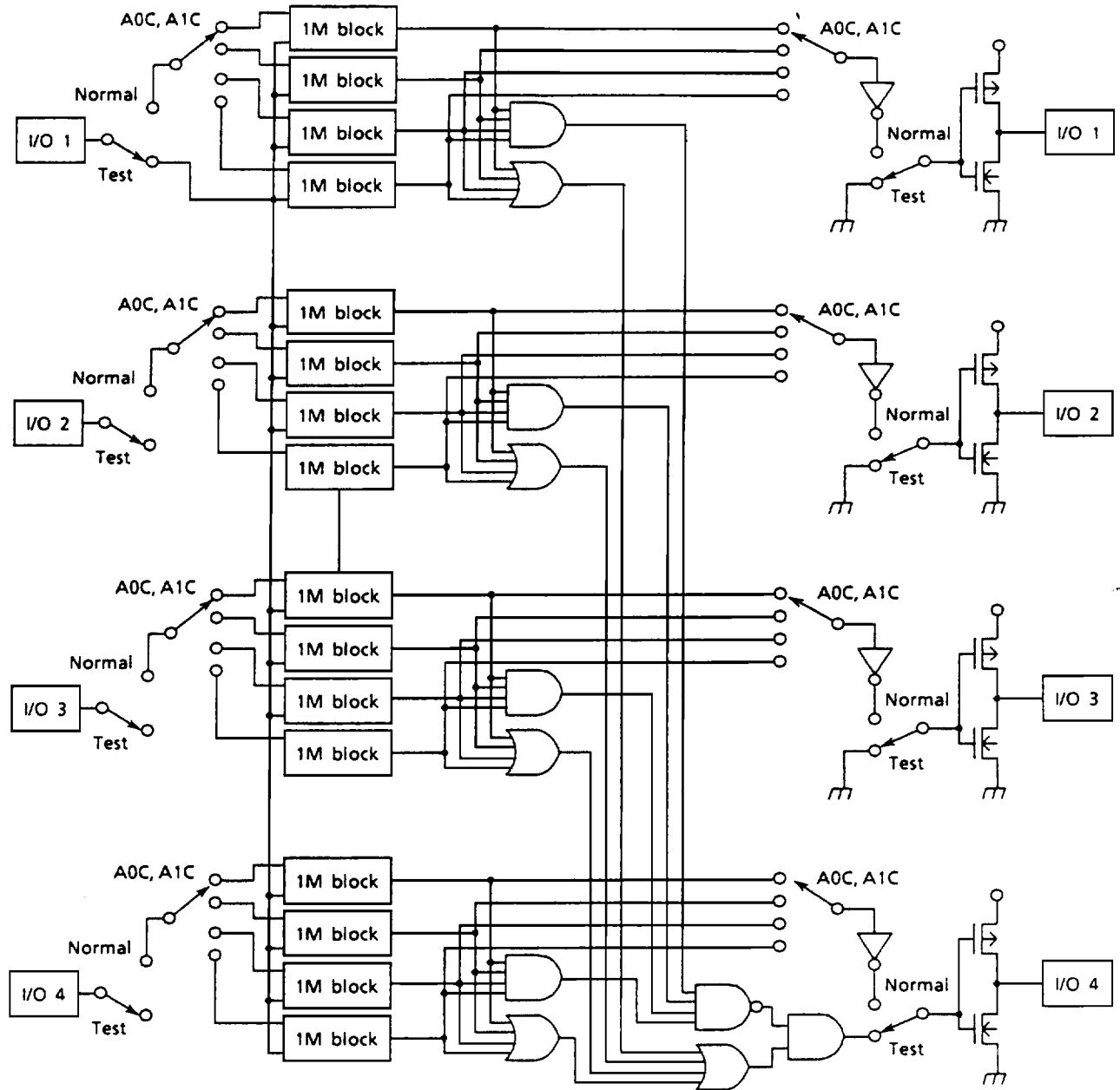


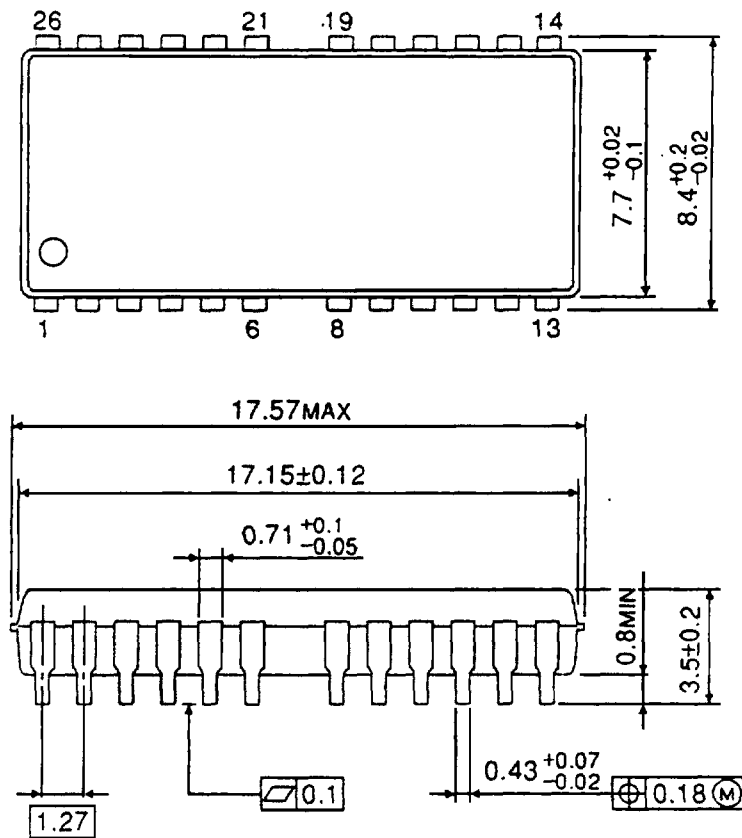
Fig. 1

INTEGRATED CIRCUIT
TOSHIBA
 TECHNICAL DATA

TC5117405 CSJ / CST - 40
 TC5117405 CSJ / CST - 50
 TC5117405 CSJ / CST - 60

OUTLINE DRAWINGS (SOJ26 - P - 300C)

Unit in mm



INTEGRATED CIRCUIT
TOSHIBA
 TECHNICAL DATA

TC5117405 CSJ / CST - 40
 TC5117405 CSJ / CST - 50
 TC5117405 CSJ / CST - 60

OUTLINE DRAWINGS (TSOP26 - P - 300D)

Unit in mm

