Triac control with a microcontroller powered from a positive supply

Introduction

This application note explains how to implement a control circuit to drive an AC switch (Triac, ACS or ACST) in case the microcontroller unit (MCU) is supplied with a positive voltage.

The driving circuit will also depends on the kind of Triac used and also if other supplies (positive or negative) are available. We also deal about the case of insulated or non-insulated supplies.

It is recommended to refer to AN4564 which explains why positive supplies are usually implemented and how simple solutions can be implemented to get a negative supply.

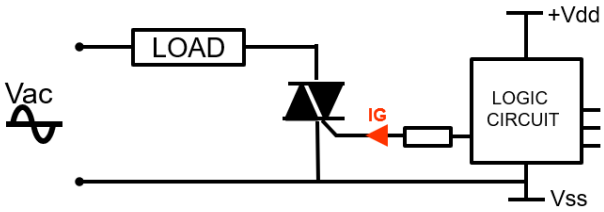
Refer also to AN3168 for information about AC switch control circuits in case the microcontroller is supplied with a negative power supply.

1 Positive supply defintion and AC switch triggering quadrants

1.1 Positive power supply

A positive power supply is a supply where its reference level (V_{SS}) is connected to the mains (line or neutral). The V_{DD} level is then above the mains terminal as shown in Figure 1. If the supply is a 5 V power supply, then V_{DD} is 5 V above the mains reference. This is why such a supply is called a positive supply (compared to a negative supply as shown in AN3168).

Figure 1. Positive supply basic schematic



1.2 AC switch triggering quadrants

To switch-on an AC switch, like any bipolar device, a gate current must be applied between its gate pin (G) and its drive reference terminal (refer also to AN3168).

Then several cases occur:

- For a SCR, this gate current has to be positive (circulating from G to K).
- For a Triac and ACST, the gate current could be positive or negative (depending on the voltage applied to the device).
- For an ACS, the gate current has to be negative (circulating from COM to G).

Four triggering quadrants can be defined according to the polarity of the gate current and the polarity of the voltage applied across the device, as shown on Figure 2.

For SCR, only a positive gate current can switch-on the device. Thus, the triggering quadrants are not considered for SCR devices.

Figure 2. Quadrants reminder (accordint to I_G direction and V_T polarity before turn-on)

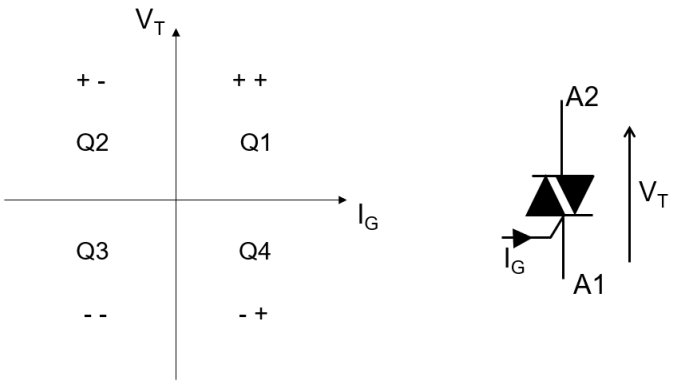


Table 1 sums-up the triggering quadrants for each STMicroelectronics AC switch family.

Table 1. Triggering quadrants for each AC switch family and class

Family	Class	Triggering quadrants			
		Q1	Q2	Q3	Q4
Triac	Standard	X	X	X	X
	Snubberless and logic level	X	X	X	N/A
	Snubberless high temperature	X	X	X	N/A
ACS/ACST	ACS	N/A	X	X	N/A
	ACST	W	W	W	N/A

Operation in quadrants Q1 and Q4 is the basic control mode which can be easily implemented with a positive power supply (cf. Section 2.1), works only with standard Triacs as shown on Table 1.

If other AC switches like ACS, ACST, Snuberless and logic level Triacs, have to be controlled by a circuit using positive power supply, as triggering in Q4 is not possible, tips have to be implemented to allow a proper operation, like it will be shown on Section 2.2.

2 In case only positive power supplies are available

2.1 Control of 4-quadrants Triacs

Standard Triacs (i.e 4-quadrant Triacs) can be controlled from positive voltage supply using simple resistor. The current will indeed flow through the gate, provided by the control IC (typically the MCU) when its I/O pin is put on a high level. When this pin is put on a low level, the Triac is no more trigerred.

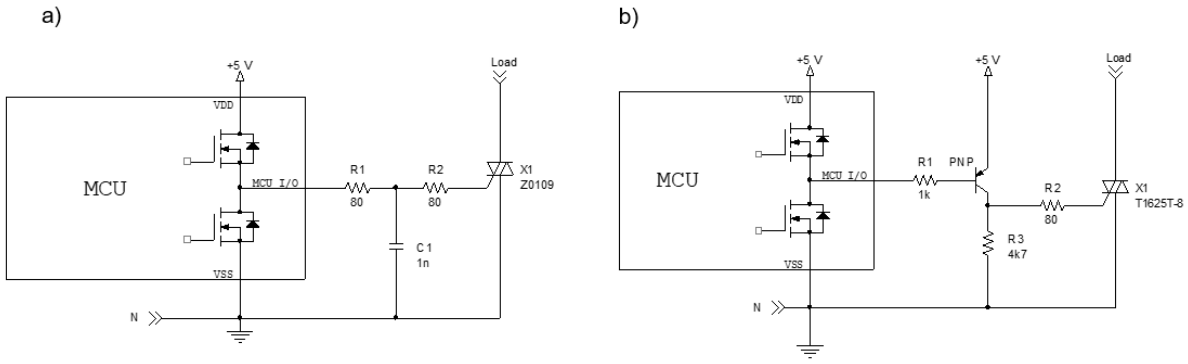
In case that the I/O port current capability of used IC is insufficient, a buffer transistor can be used to amplify the gate current.

Figure 3 a) gives an example of a gate circuit with a direct MCU control. The R1-C1-R2 filter circuit is used to improve the immunity of the controlled Triac or of the control IC. In Figure 3 a), C1 and R2 can be removed in the circuit as the immunity is high enough without these components.

Please note that R2 is required to prevent Triac damage in case of turn-on with high dI/dt as it is explained in AN4030.

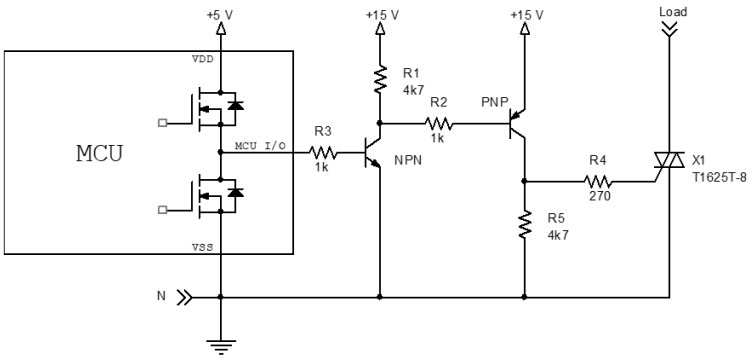
Figure 3 b) gives an example of a gate circuit with a buffer transistor.

Figure 3. Gate circuits for 4-quadrant Triacs from positive voltage control



The circuit with a bipolar transistor is also particularly interesting if a second level supply is available. Indeed, such a second voltage level supply may already be available for supplying other devices like relay coils, power LEDs or small actuators. Then a direct supply from MCU is not desired if the MCU power supply features a low current capability. But this could be also the case if the MCU I/O pins features a low current sourcing capability. Such a schematic is shown on Figure 4.

Figure 4. Gate circuit of 4-quadrants Triacs from two level positive voltage control



2.2 Control of 3-quadrants Triacs

Three quadrant devices (Snubberless Triac, high temperature Triacs, ACST devices) cannot be controlled directly from a positive power supply. A capacitor can then be used to provide a negative current. Two main strategies only exist, one with R-C circuit and the other one with R-C circuit including a diode.

2.2.1 Control strategy with R-C circuit

In case only a single positive voltage for IC (MCU) is available the Triac can be controlled directly from I/O port (refer to Figure 5) if a capacitor (C1) is added in series with the gate resistor (R1).

The principle of operation of Figure 5 a) schematic is the following one (refer also to Figure 6):

- When the MCU I/O pin is put to a high level (V_{DD}), capacitor C1 is charged through R1 and the Triac gate. As a 3-quadrants Triac could not be triggered in quadrant Q4, the Triac will not turn on if the voltage across terminals A2 and A1 (referenced to A1) is negative (but could turn-on if this voltage is positive, in Q1 quadrant mode).
- When C1 capacitor is fully charged (to MCU supply which is 5 V here) the current disappears.
- When the MCU I/O pin is put to low level (V_{SS}), C1 is discharged through R1 providing a negative current to the Triac gate. The Triac is then triggering in Quadrants Q2 or Q3 respectively if the voltage across its terminals is positive or negative. The negative current flows until the capacitor C1 is discharged.

Figure 5 b) gives a variant of Figure 5 a) schematic for the specific case to control an ACS device. Indeed such devices present a single P-N junction between their COM and G terminals which prevent any current flow source from G to COM. D1 diode is then added to allow the charge of C1 capacitor when the MCU I/O pin is put at high level.

Then, as shown on Figure 6, an alternative gate current is applied as long as the MCU I/O pin applies a burst voltage pulse.

The advantage of such a control method is that the capacitor blocks the DC current that can appear in case of IC circuit failure like reset, latch-up etc. It means increased safety level of the application.

Figure 5. Gate circuit of direct MCU control (a: 3-quadrants Triacs or ACST, b: ACS)

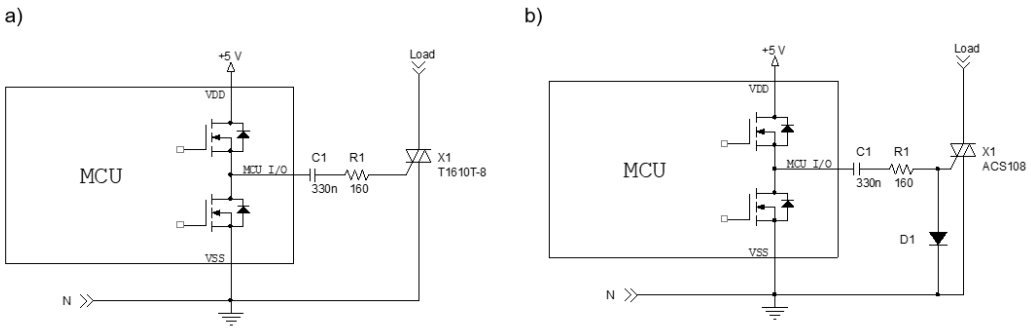
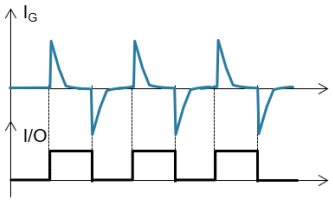


Figure 6. Gate control principle

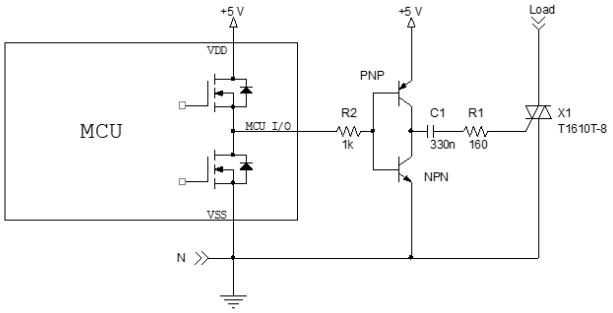


The solution is suitable especially for control of sensitive devices, typically I_{GT} = 5, 10, 20 mA due to a limited I/O port capability and IC circuit capability.

In case a higher gate current is requested, a push-pull circuit can be used (refer to Figure 7). The advantage of this solution is that the necessary gate current is not stressing the IC with excessive current.

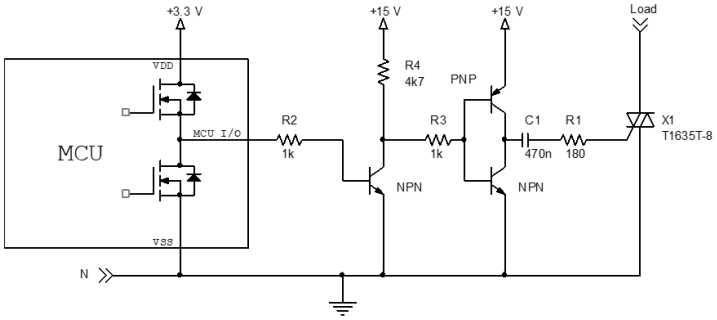
For sure, PNP and NPN bipolar transistors can be replaced respectively by a P-channel and an N-channel MOS transistors to reduce the IC current consumption.

Figure 7. Push-pull gate circuit for single level supply voltage



In case the positive power supply has two output voltages (typically +15 V, +3.3 V) the push-pull circuit can be used if the control IC is not able to withstand a supply from a higher voltage level (refer to Figure 8). The advantage of this solution is that the current capability of the IC power supply can be lower.

Figure 8. Push-pull circuit for two level supply voltage



The principle of operation of Figure 7 and Figure 8 circuits is basically the same than Figure 6 one, except that, for Figure 7, the MCU I/O pin has to be put at a high level to discharge C1 and sink a current from the Triac gate.

2.2.2 Control strategy with R-C circuit and diode

In case a gate current amplifier is requested, a simpler solution than the push-pull circuit is presented on Figure 7. This circuit uses a simple diode instead of another transistor as shown in Figure 9 and Figure 10.

The solution of Figure 10 is mandatory for ICs with only open-drain outputs. For sure it works well if the I/O pin can be configured in push-pull.

Figure 9. Basic diagram of the gate with R-C circuit and diode

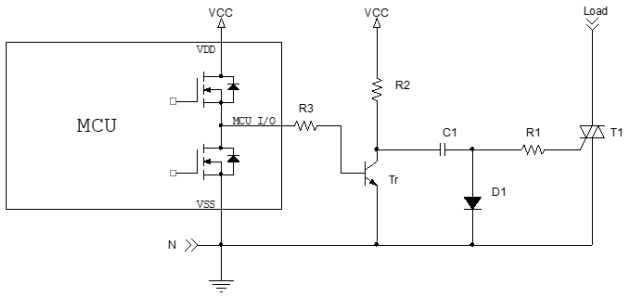
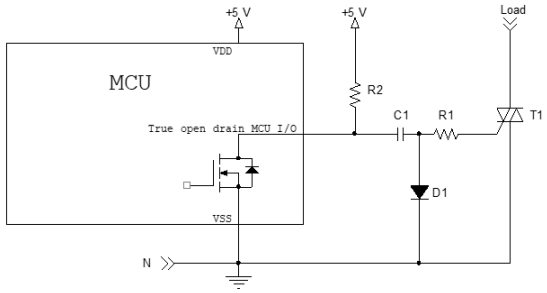


Figure 10. R-C-D circuit implemented with true open-drain I/O



The principle of operation of both circuits is the following one (we take into account Figure 9 components references in below text):

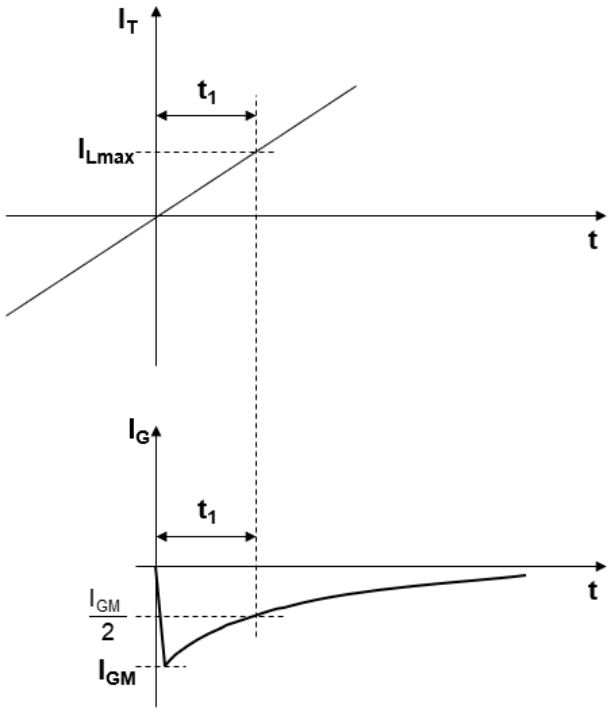
- When Tr transistor is switched-off, capacitor C is charged through R2 resistor and D diode. The diode is used to faster charge the capacitor and avoid that the charging current is limited by R1 resistor too. A Schottky diode could be used to keep the voltage drop level below the gate non trigger voltage (V_{GD}). This also avoids to apply a positive gate current to the Triac when Tr is OFF, and avoids to spuriously trigger it.
- When the Triac has to be triggered, T_r transistor is switched-on, C is discharged through R1 and T_r and a negative current flows through the Triac gate.

2.2.3 Gate pulse width setting

The Triac latching current (I_L) is the minimum value of the load current which allows the device to remain in the conducting state after the gate current I_G has been removed. In general the gate current must be kept at least above I_{GT} level until the load current reaches this latching current level to ensure a proper turn-on (as explained in Figure 11).

This minimum gate current pulse (t) could be quite long then in case of low RMS current loads.

Figure 11. Gate control principle



The time t1, required by the load current to reach the maximum latching current level, in case of sinusoidal waveform, is given by following equation:

$$t_1 \geq \frac{1}{\omega}\text{asin}\left(\frac{I_L\,\text{MAX}}{I_{\text{RMS}} \cdot \sqrt{2}}\right) + 10\mu\text{s} \quad \text{and} \quad t_1 \geq 20\,\mu\text{s} \tag{1}$$

Where: ω = 2.π.f and f is mains frequency.

I_{RMS}: minimum RMS current of the load (depending on line and load variations).

The 10 µs time is added to ensure a minimum duration of the gate pulse and to take into account other circuits delays (typical turn-on time of the Triac, MCU accuracy, etc.).

To ensure a minimum pulse width, it's better to limit t_1 time to at least 20 µs in case the calculated value with above the equation is too low.

It should be noted that Triac latching current depends on the triggering Quadrant. With Section 2.2 circuits, the triggering quadrants are Q2 or Q3.

Then, the latching current will depend on the selected part-number.

For example, for most of 35 mA Snubberless Triacs, the specified latching currents are:

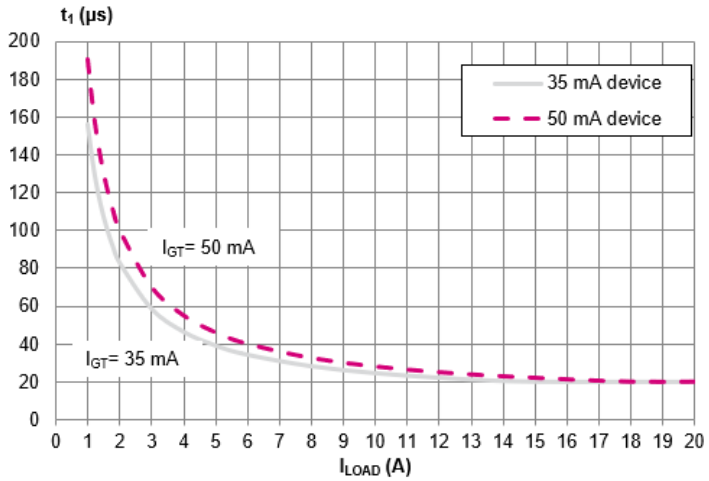
- Q1 and Q3: I_L max = 60 mA
- Q2: I_L max = 65 mA

And for most of 50 mA Snubberless Triacs, the specified latching currents are:

- Q1 and Q3: I_L max = 70 mA
- Q2: I_L max = 80 mA

Figure 12 shows the minimum time versus the RMS load current for a 50 Hz application for these two Triacs families.

Figure 12. t_1 time versus RMS load currents (worst case: I_L Q2)



2.2.4 Gate control circuits design

We have to consider two main parameters to define all the components of Section 2.2 gate control circuits:

- The TRIAC gate triggering current (I_{GT})
- The TRIAC latching current (I_L) (as explained in previous section).

I_{GT} is the maximum gate trigger current specified in the Triac datasheet. To ensure a good safety margin and a good triggering we chose a peak gate current (I_{GM}) two times higher than the I_{GT}.

Also in order to take into account that the I_{GT} increases when the junction temperature decreases, we take into account the gate current level for a 0 °C junction temperature which is usually the lowest ambient temperature for most appliances. In case of operation at a lower temperature, the gate current increase factor has to be extracted from the Triac datasheet curve, for the specific working temperature.

The gate resistor can be then defined by the following equation:

$$R1 = \frac{V_{CC} - V_{GK} - V_{CE}}{2 \times I_{GT}(0°C)} \quad (2)$$

Where V_{CE} is the saturated voltage of the control transistor or the max V_{OL} voltage of the I/O pin at low-level in case of direct control by a MCU (Figure 5 and Figure 10 schematics).

Typically V_{CE} = 0.2 V and V_{GK} = 1.3 V at I_{GM} = 2 . I_{GT}

Capacitor C1 is then given by the following equation to ensure that the applied gate current will remain above I_{GT} at the end of the previously defined t1 pulse time.

$$C1 \geq \frac{t_1}{R1.\ln(2)} \quad (3)$$

In case an open-drain circuit is used as explained in Section 2.2.2 , to ensure that capacitor C will be charged for the next half cycle (in case a pulse is applied only at each half-cycle), R2 should be chosen with below equation where the charging time constant is set lower than 1 ms:

$$R2 < \frac{0.001}{C1} \quad (4)$$

Figure 13 gives a typical oscillogram within the following conditions:

- Controlled device : ACST610-8T
  - I_{GT}= 10 mA
  - I_L max Q2 = 40 mA
  - I_L max Q1-Q3 = 30 mA
- Line voltage: 230 V RMS, 50 Hz
- Load RMS current: 4 A (load power: ~900 W)
- V_{CC} = 5 V
- R1 = 160 Ω
- C1 = 470 nF
- t_1 = 200 µs

The control circuit is the one shown on Figure 5 or Figure 7.

Figure 13. R-C circuit triggering at zero current for a) positive polarity b) negative polarity

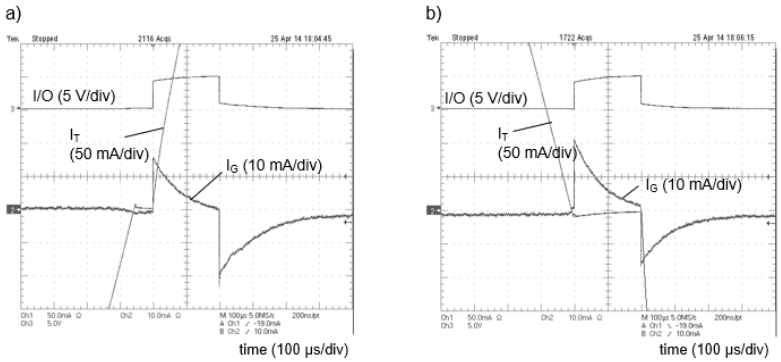


Figure 13 a) shows that the Snubberless device can be triggered in positive polarity with the first positive gate current pulse applied during the rising edge for the MCU I/O output signal (Q1 quadrant). The negative gate pulse (Q2 triggering) is then not useful.

Figure 13 b) shows that the Snubberless device cannot be triggered in negative polarity by the positive gate current pulse as Q4 triggering is prohibited for such devices. But the device is then well triggered with the negative pulse (Q3 triggering). As voluntary shown in this figure (with a gate pulse applied with a small delay to highlight the non-triggering in Q4), there could be a short zero-current operation in case the pulse is not well synchronized with the load zero current event. Such issue could be solved with an enlarged gate pulse. In case, the load zero current event time is not known, a gate burst has to be applied as shown in Figure 6).

Figure 14 gives a typical oscillogram when an open-drain circuit is used like explained in Section 2.2.2 (cf. Figure 9 and Figure 10), within the following conditions:

- Controlled device : T1610T-8FP
- Line voltage: 230 V RMS, 50 Hz
- Load RMS current: 4 A (load power: ~900 W)
- V_{CC} = 5 V
- R1 = 160 Ω
- R2 = 1.2 kΩ
- C1 = 470 µF

In this Figure, it is shown that just the negative part of C1 current is sunk from the gate. The positive part is derivated by D1 diode and then is not applied to the gate.

Figure 14. Triggering at zero current with open-drain circuit

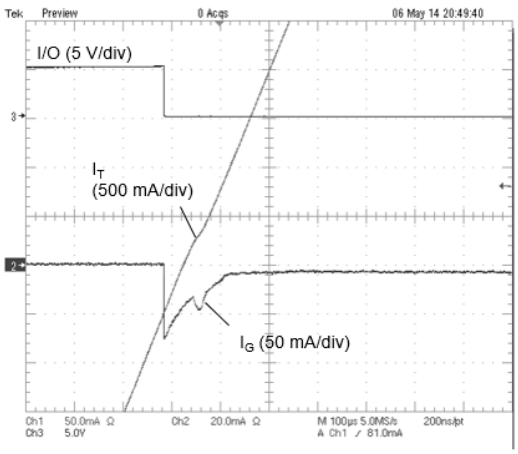


Table 2 shows the influence of the Triac/ACS switch sensitivity and of the supply voltage on the R1-C1 circuit values. The values are calculated for a 5 A RMS current. For sure, for a lower load current, the pulse width has to be larger as shown on Figure 12.

10 mA and 20 mA devices can be controlled directly from 5 V supply as the capacitor value remains below 1 µF that is maximum value for standard 0805/0603 /16 V SMD capacitor.

For 35 mA, required C1 capacitor is 2 µF for a 5 V supply. Using a higher voltage (typically 15 V) will allow a higher charge to be stored with a small capacitor value. Using a 15 V supply instead of 5 V allows then a capacitor value decreased by a factor 3-4.

Table 2. Variation of the RC parameters with V_{CC} for different triac sensitivity

Sensitivity	I_{GT} = 10 mA		I_{GT} = 20 mA		I_{GT} = 35 mA	
Supply voltage	V_{CC} = 5 V	V_{CC} = 15 V	V_{CC} = 5 V	V_{CC} = 15 V	V_{CC} = 5 V	V_{CC} = 15 V
I_L(mA)	30	30	40	40	65	65
t_1(µs)	24	24	28	28	39	39
R1(Ω)	120	470	62	240	36	130
C1(nF)	470	100	820	220	2000	680

Table 3 shows the limitation of this control method. The capacitor value is increasing fast when the load current decreases. Higher supply voltage could help to reduce the capacitor value as previously explained.

These control methods are then suitable for mid and high power loads without high variation of the load current.

Table 3. Component values for R-C circuit with diode for different I_{RMS} and V_{CC} = 5 V for 35 mA device

	I_{RMS} = 2 A	I_{RMS} = 5 A
$t_1$min(µs)	77.5	37
R1 max(Ω)	30	30
C min(µF)	3.8	1.8
R2 max(Ω)	263	555

3 MCU supplied by a positive supply but a negative supply is available

3.1 Triac choice

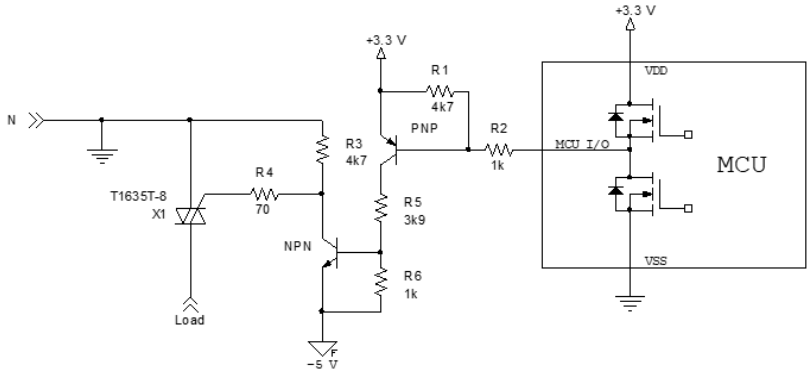
In applications where a negative non-insulated power supply is available, the Triacs can be controlled with negative voltage i.e. in Q2-Q3 quadrants that is suitable for control of all types of Triacs and AC switches. Three-quadrant triacs are preferred (refer to AN3168) due to the better dynamic performance compared to standard 4-quadrant Triacs.

3.2 Non-insulated supplies

Some applications with low power DC loads like BLDC motor with output power below ~50 W and AC loads use half-wave rectification. Positive power supply is necessary for BLDC motor control. But there are simple SMPS solutions which allow to implement both a positive and a negative supply. The negative power supply can then be used for a Triac control.

Figure 15 gives a simple level-shifter circuit which can then be used in this case to allow Triacs control from the negative supply while the IC is supplied from the positive supply.

Figure 15. Control circuit for non-isolated positive and negative power supplies



R4 is chosen according to the sensitivity of the controlled Triac and supply voltage (here -5 V is used in this example).

R5 has to be chosen according to the used supply voltages and to ensure proper saturation of the NPN transitor. To provide approximately 100 mA to the Triac gate, and considering a low amplification gain (β~ 50 for the NPN transistor), a 3.9 kΩ value can be used for R5.

R6 is used for better immunity and stability.

3.3 Insulated supplies

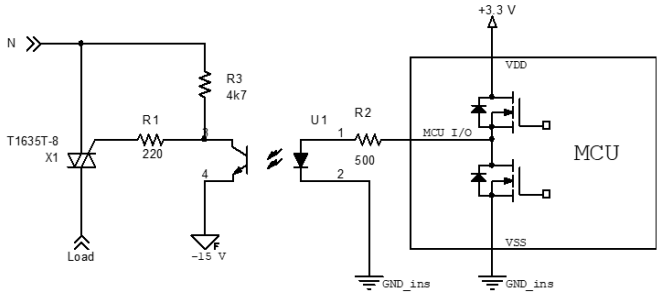
Insulated power supplies are used to supply the MCU of several applications for different reasons (the MCU is connected to basic-insulated sensor which can be touched by an end-user; the MCU is referenced to the low-level of the DC bus behind a diode bridge; etc.).

In that case, as the Triac control reference is connected to one terminal of the AC mains, it must be controlled with an isolated circuit and supplied from a supply insulated from the MCU one.

A circuit with opto-transistor is preferred to an opto-Triac solution as the Triac gate pulse duration can be accurately controlled. The added cost of the auxiliary supply (need for Triacs gate current supply) can be alleviated if different Triacs are used and then use the same power supply.

Figure 16 gives such a control circuit schematic with an opto-transistor solution.

Figure 16. Opto-transistor control circuit



Gate resistor R1 is chosen according Triac sensitivity and supply voltage, here the -15 V is used as example. R3 is not mandatory but it improves the Triac EFT immunity as the gate is not floating during the time when gate pulse is not present. Lower value of R3 will have higher impact to immunity but increase the current consumption. R2 must be chosen with respect to opto-transistor current transfer ration (CTR) to reach sufficient gate current. R-C-R gate circuit, as shown in Figure 3, can also be used here.

4 Conclusion

Different solutions have been presented to control an AC switch (Triac, ACS or ACST) in case the microcontroller unit (MCU) is supplied with a positive voltage.

Anyway, the use of a negative supply is recommended as it allows an easier replacement of an AC switch by another one (for example, an ACST can be used in place of a standard Triac without requiring to modify the whole control circuit). Moreover, the triggering in Q4 is not advised because the triggering gate current is the highest, therefore it may cause a higher board consumption.

Refer to AN3168 for further information on AC switch control circuits where the microcontroller is directly supplied with a negative power supply.

Revision history

Table 4. **Document revision history**

Date	Version	Changes
May-1992	1	Initial release.
23-Apr-2004	2	Style sheet update. No Content change.
10-May-2008	3	Reformatted to current standards. Full technical review.
20-Mar-2020	4	New version with different configurations of Triac drivers.

Contents

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